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# A Survey on Reversible Logic based LFSR

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## ABSTRACT

Reversible logic has emerged as one of the most important approaches for the optimization of power in low power VLSI design. They are also the basic requirement for the emerging field of the Quantum computing having their applications in the areas such as Digital Signal Processing, Nano-Technology, Cryptrography etc. It means performing computation in such a way that any previous state of the computation can always be reconstructed with given description of the current state. Here Reversible logic is used for designing a Linear Feedback Shift Register (LFSR). LFSR is a shift register that, when applied with the clock, shift the signal through the register from one bit to the next most-significant bit. Outputs from some of the register are combined through the exclusive-OR configuration and feedback mechanism is formed. Linear feedback shift register can be formed by performing exclusive-OR on the outputs of two or more of the flip-flops together and feeding those outputs back into the input of one of the flip-flops. As a prior work, literature survey has been done.

**Key words:** Reversible logic, Quantum Computing, Linear Feedback Shift Register.

## INTRODUCTION

Reversible Logic has received great attention in the recent years due to their ability to reduce the power dissipation which is the main requirement in low power VLSI design. Quantum computers are developed using reversible logic circuits. In 1960 R. Landauer showed that, circuits and systems of high technology constructed using irreversible hardware result in energy dissipation due to information loss. According to him, the loss of one
bit of information dissipates at least KTln2 joules of energy, in which K refers to Boltzmann's constant and T is the absolute temperature at which the operation is performed. In 1973 Bennett showed that, one can avoid KTln2 joules of energy dissipation by designing the circuits using reversible logic gates.

Here Linear Feedback Shift Register (LFSR) will be designed using reversible logic in order to reduce the power dissipation which generates pseudo random signals used in Built-In-Self-Test(BIST). Since BIST is the most suitable approach for low power testing as it provides a larger scope for low power techniques to be used. BIST uses LFSR as test pattern generator (TPG). The LFSR generates all possible test vectors with the proper use of tap sequence. Furthermore the pseudo random behavior of the LFSR reduces the correlation among the test vectors which means that it can achieve high fault coverage in a relatively short run of test vectors. It is therefore required to find an optimum linear feedback shift register which, itself is power efficient and the test vectors generated are also power efficient.

## LITERATURE SURVEY

In this section, detailed literature review is done that aims to review the critical points of current works. Here the information collected about researches and innovations carried out on the related technologies has been done. This section will highlight the recent trends and innovations in the concerned technology.

Landauer [1] determined that, the amount of energy dissipated for the loss of each bit of information is at least kTln2 (where k is the Boltzmann constant i.e. 3 *10^12 joule at room temperature). During any computation the intermediate bits used to compute the final result are lost, this loss of bits is one of the main reason for the power dissipation.

C. H. Bennett [2] in 1973 discovered that the power dissipation in any device can be made zero or negligible if the computation is done using reversible model. The theory is proved with turing machine which is a symbolic model for computation developed by Turing. Bennett also showed that the computations that are performed on irreversible or classical machine can be performed with same efficiency on the reversible machine. Based on the above concept the research on the reversibility was started in 1980's.

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Mozammel H A Khan [3] has illustrated an ALU using reversible logic and explained that reversible circuits dissipate less heat than the irreversible circuits. Here the author embedded an n-bit classical ALU on reversible circuits which can perform both arithmetic and logical operations on n-bit data.

Another computing paradigm is quantum computing. All reversible gates have their corresponding quantum version. This implies that, all reversible circuits can be realized as quantum circuits.

Soolmaz Abbasalizadeh[4] has designed 4-Bit Comparator Based on Reversible Logic Gates. Here he explained that reversible logic has been considered as one of the promising practical strategies for power-efficient computing. In fact, when the inputs can't be recovered from circuit's outputs, information loss appears. Reversible logic circuits can handle this issue. In this logic, one to one mapping exists between the inputs and outputs. The number of inputs and outputs are equal, and inputs can be recovered from outputs. In order to achieve optimized reversible circuits, the following points should be considered:

1) Fan-out is forbidden.
2) Feedbacks and loops are not allowed.
3) Delay should be minimum.
4) Optimization parameters should be minimum.

The parameters such as number of reversible gates, number of constant inputs, garbage outputs and quantum cost can be named as optimization parameters and are defined as:

1) The inputs, which equal to 0 or 1, are constant inputs.
2) Garbage outputs are output vectors which do not generates any use full functions.
3) Quantum cost refers to the cost of the circuits in terms of primitive gates.

Arunkumar P Chavan[5] has proposed the pulse detector and unsigned multiplier. He also explained the 4-Bit reversible PISO Shift register. Here the 4-bit PISO shift registers uses four reversible clocked D flip-flops and four Fredkin Gates. Reversible Fredkin Gate is used to develop a multiplier with an enable signal. Similarly a basic 3-bit reversible SIPO shift register can be constructed using three reversible clocked D flip-flops and two Feynman Gates.

Praveen J and M N Shanmukaswamy[6] have proposed new power reduction technique in LFSR using modified control logic for VLSI circuit. It is explained that LFSR is a proposed technique which targets to reduce the power consumption in the BIST. The power consumption is reduced during testing of a circuit under test (CUT) in two stages of testing. At first stage, control logic (CL) makes the clock of the switching units of the register inactive for a period of time, when the output from them is same as previous output and thus reducing the switching of the flip-flop. And at the second stage, LFSR reorders the test vectors by interchanging the bits with its next and closest neighbor bit. It keeps fault coverage capacity of the vectors unchanged but reduces the Total Hamming Distance (THD) so that there is a reduction in power while shifting operation.

However, the vector ordering can be used in BIST also. In ordering techniques, the THD that is the sum of the hamming distance is minimized by modifying the order in which test vectors of a sequence are shifted into the CUT. The test vector ordering has been useful in minimizing the hamming distance among the test vectors and thereby reducing in average and peak power.

Mohd. Marufuzzaman, L. F. Rahman and H. Hussain[7] have illustrated that, LFSR is key component to provide self-test of an integrated circuit (IC). This research is implemented LFSR until layout level which forms the key point for low power application. The paper shows the LFSR as well as D flip flop using various architecture in a 0.18μm CMOS technology so that the layout area will be minimized as well as the power consumption will be lower.

LFSR systems are typically designed either using field programmable gate arrays (FPGAs) or digital signal processors (DSPs). While this leads to a working system which are flexible in nature, then the system speed is limited by the fact that FPGAs and DSPs are all general-purpose systems. By using VLSI techniques in order to come out with the design of a LFSR, the throughput can be increased and the LFSR is easily integrated into a system design since the area needed is minimal. This research presents three different automated techniques for implementing LFSR as well as D flip flop so that the layout area will be minimized as well as the power consumption will be lower.

M. Janaki Rani[8] proposes a low leakage power linear feedback shift register that can be used in a crypto-processor. This paper also proposes two

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leakage reduction techniques such as reverse body bias and transistor stack, which are applied to the circuits. Leakage power makes up to 50% of the total power consumption in today's high performance microprocessors. Therefore leakage power reduction becomes the key to a low power design.

The leakage current flowing through a stack of series connected transistors reduces when more than one transistor of the stack is turned OFF. The effect is called as "Stacking Effect". When two or more transistors that are switched low or OFF, and are grouped that are put one on top of each other then they dissipate less leakage power than a single transistor that is turned OFF which reduces the leakage current.

Reverse body biasing (RBB) can be used to dynamically raise the threshold voltage during standby mode, thereby reducing the leakage power. Reverse bias is applied to the body of the devices and threshold voltages can be changed which is due to the body effect. For example, biasing an NMOS device body with a voltage lower than Ground, or biasing a PMOS device body with the voltage higher than Vcc will increase the threshold voltage which results in reduction in leakage current.

## CONCLUSION

The main aim is to design and implement the reversible logic based LFSR. As a prior work, literature survey has been done. It is observed that, there are many innovative ideas and solutions are put forth for the power optimization by many researchers such as reverse body bias, transistor stacking, LFSR design with parallel architecture, pipelining and retiming algorithms and reversible logic.

So observing all these white papers, one can ensure that reversible logic would be one of the better solutions for the designing of LFSR in order to generate the pseudo random signals, with the better optimization of the power.

## REFERENCES

[1] Landauer .R, *"Irreversibility and heat generation in the computing process"*. IBM J. Research and Development, pp. 183-191, 1961.

[2] Bennett C.H., *"Logical reversibility of Computatio"*. IBM Research and Development, pp. 525-532, 1973.

[3] Mozammel H A Khan., *"Classical Arithmetic Logic Unit Embedded on Reversible/Quantum circuits"*. IEEE transaction 2012.

[4] Soolmaz Abbasalizadeh., *"4-Bit Comparator Deign Based on Reversible Logic Gates"*. IEEE transaction 2013, volume1, no3

[5] Arunkumar P Chavan., *"Design of Pulse Detector and Unsigned Sequential Multiplier using Reversible Logic"*. International journal on computer application, volume92, no 4, April 2014.

[6] Praveen J, M N Shanmukaswamy *"Power Reduction Technique in LFSR using Modified Control Logic for VLSI circuit"*. International journal of computer application 2012.

[7] Mohd. Marufuzzaman,*"design of low power linear feedback shift register"*. Journal of Theoretical and Applied Information Technology. 20th March 2014. Vol. 61 No.2.

[8] M. Janaki Rani , S. Malarkan.*" Design and Analysis of a Linear Feedback Shift Register with Reduced Leakage Power"*. International journal of computer application volume 56- no 14, 2012.

[9] Praveen kasunde, Dr. K B Shivakumar and Dr M Z Kurian,*" Improved design of low TPG using LP-LFSR"*, international journal of computer and organization trends-volume3 issue4-may 2013.

[10] Chao Cheng, Keshab K. Parhi, *"high speed VLSI architecture for general linear feedback shift register structures"*. IEEE transaction 2009.

[11] Saurabh Kotiyal, Himanshu Thapliyal, *"circuits for reversible quantum multiplier based on binary tree optimizing ancilla and garbage bits"*, 27th international conference on VLSI design IEEE transaction 2014.

[12] Zhijin Guan, Wenjuan Li, *"An Arithmatic Logic Unit Design Based on Reversible Logic Gates"*, IEEE transaction 2011.