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Design of basic CMOS Buffer and Enhanced Low Power CMOS Buffer

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Abstract: ***Buffers are widely employed in digital circuits where high speed signals are used. In this paper we are going to design basic CMOS Buffer, which is noisy, and an enhanced CMOS Buffer which is less noisy. We also design low power enhanced CMOS Buffer by using different foundries. Power dissipation of the enhanced CMOS Buffer's is compared and the one with low power is suggested.***

Keywords: ***Buffer, Enhanced Buffer, CMOS, Power.***

I. INTRODUCTION

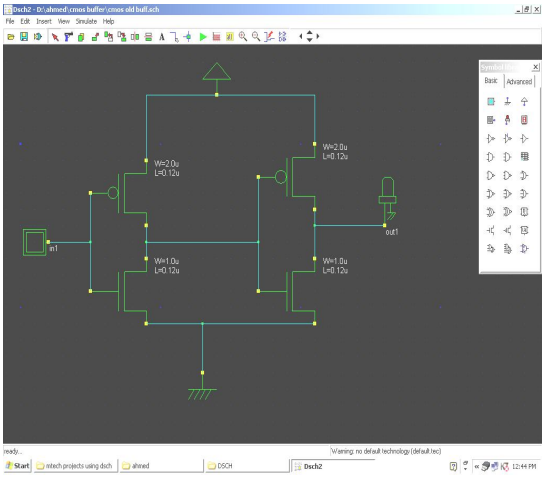
Buffer: It is the device which is widely used in transmission of information along the interconnection lines to multiple receivers. It is used for incrementing the driving capability of given logic signal for huge load capacities. Buffers are used for a circuit with large fan-out to reduce the delay of entire circuit.

Buffers are useful when there is a difference between the rate at which data is received and the rate at which it can be processed. The data has to be modified before it is read or write with input and output data in sequential manner. In Oscillatory circuits CMOS buffer can be used. CMOS circuits have high gain, high input impedance, high bandwidth.

CMOS devices have a high input impedance, high gain, and high bandwidth

II. IMPLEMENTATION

The basic CMOS circuit is designed as shown below it consists of 2 pmos transistors and 2 nmos transistors along with power supply V_{DD} and ground, with input as in1 and output as out1.



Below figure is with no input applied

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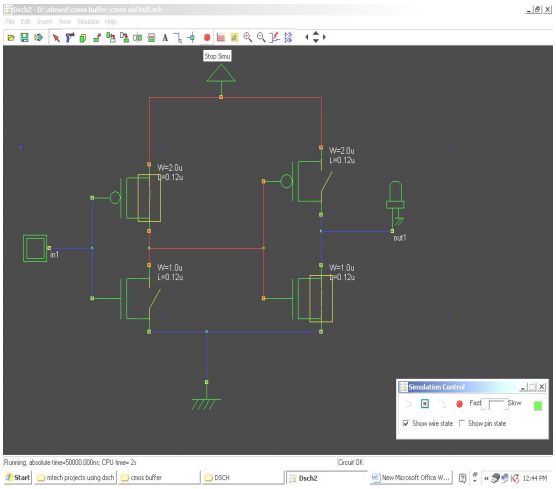
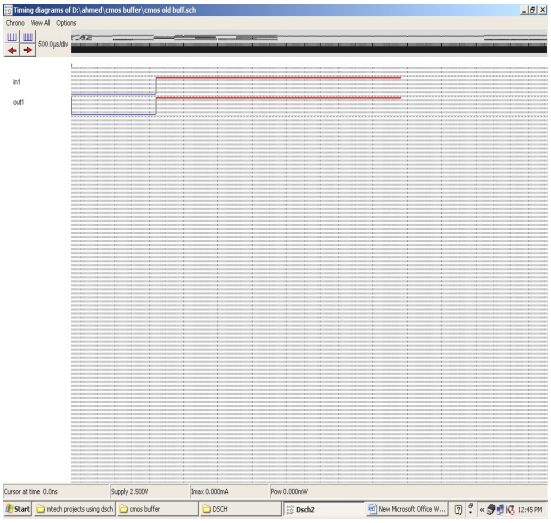
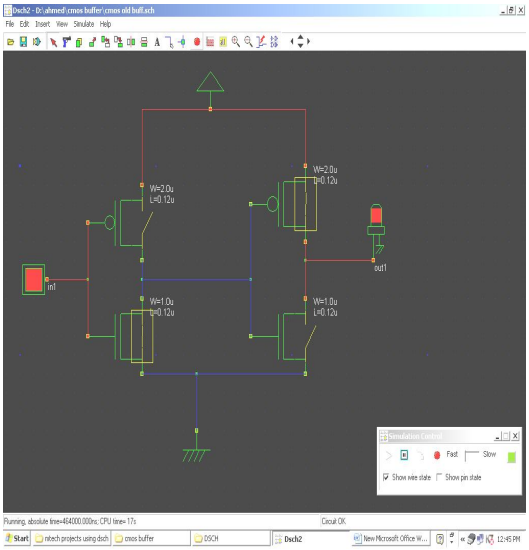




Below figure is with input applied

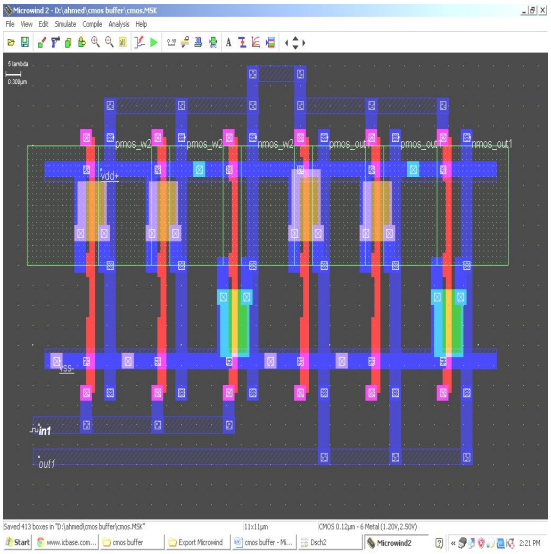


The corresponding analog simulation graph is as

Shown below

The corresponding circuit layout with 0.12µm technology and analog simulation is as shown below.

Layout:



Analog Simulation:

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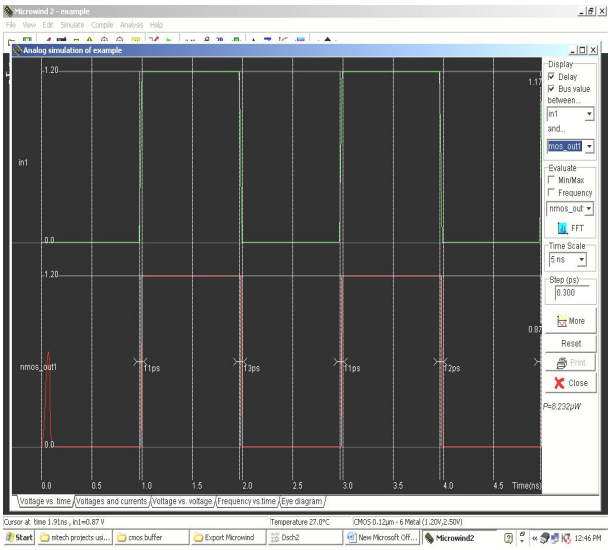
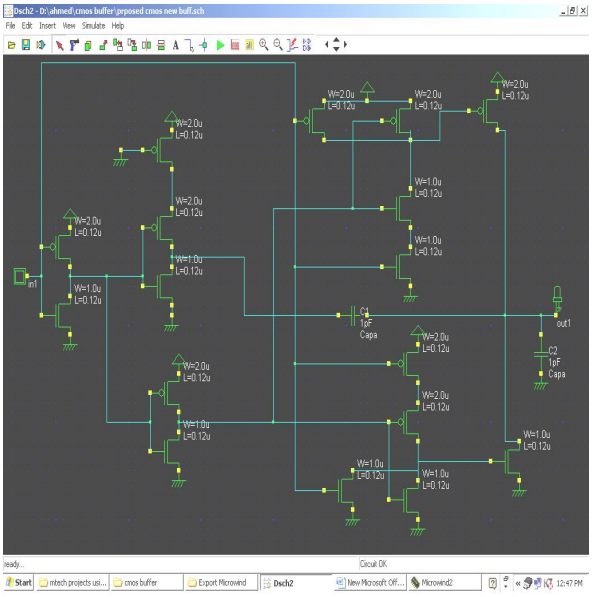
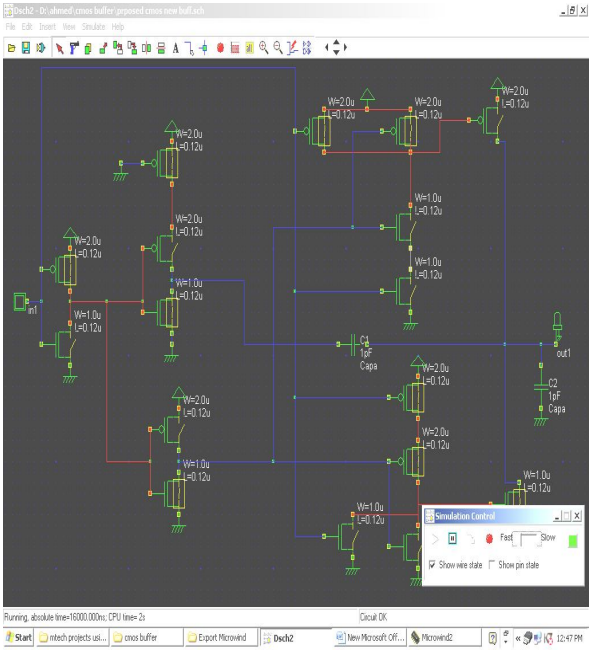




Below figure represents Enhanced CMOS buffer with no input

The new proposed enhanced CMOS buffer designed is as shown below we add a group of serial 2 PMOS gates, with 2 NMOS gate, and an Inverter connected from first stage output. In the second stage the two PMOS gates are connected parallel with 2 NMOS gates and 2 serial PMOS gates connected to 2 parallel NMOS gates from the output of Inverter. From here the outputs are connected to final stage and output



Below figure represents Enhanced CMOS buffer with input

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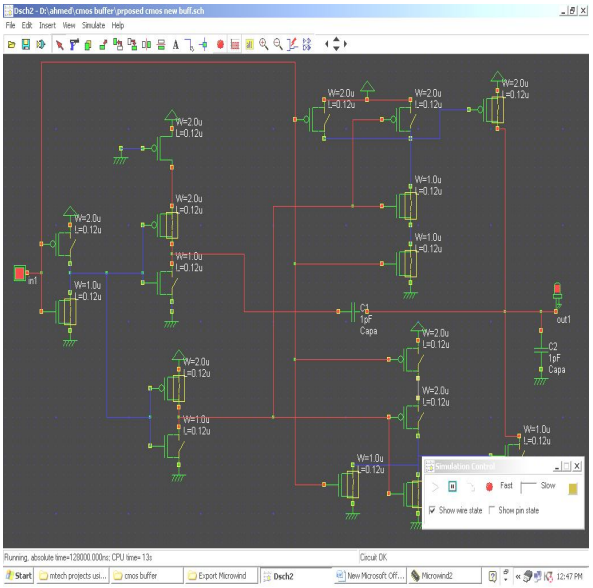
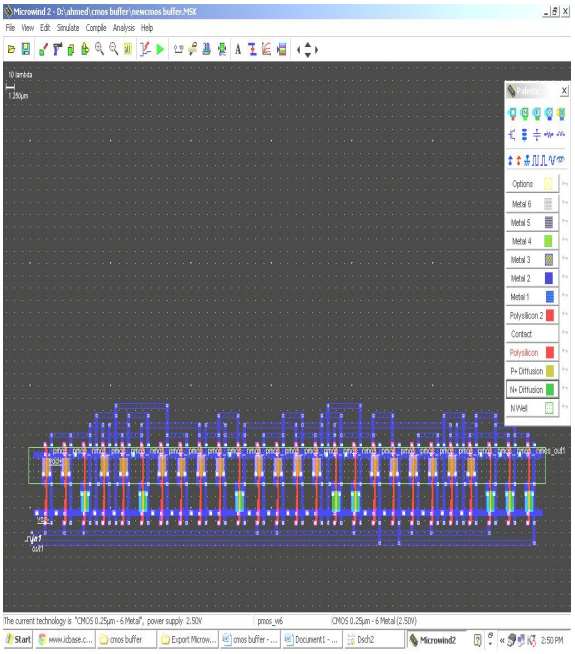
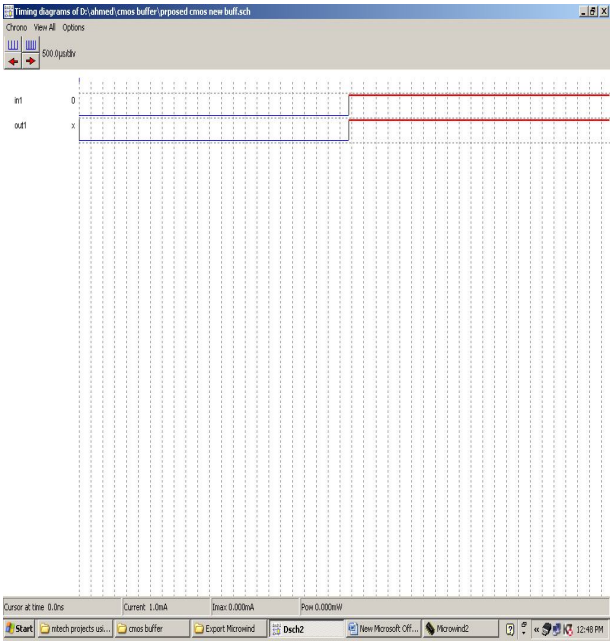
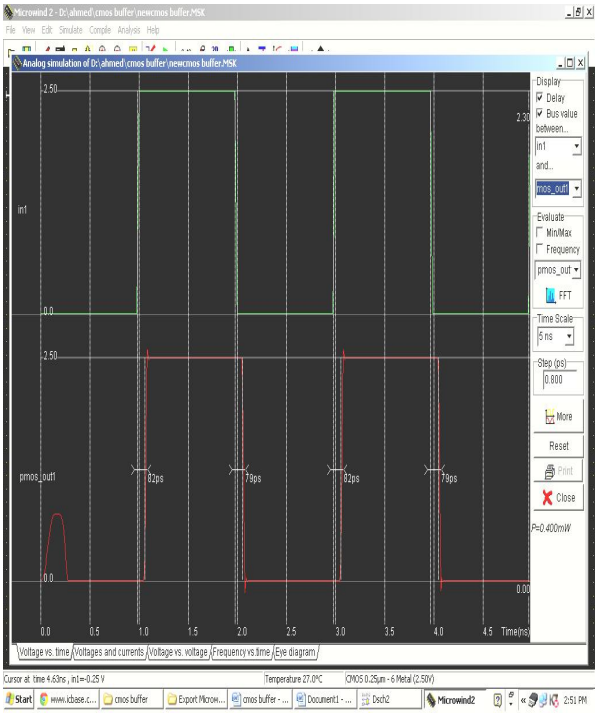




Corresponding graph of enhanced CMOS buffer is as shown below





The Layout with 0.25µm technology and analog simulation of enhanced CMOS buffer is shown below

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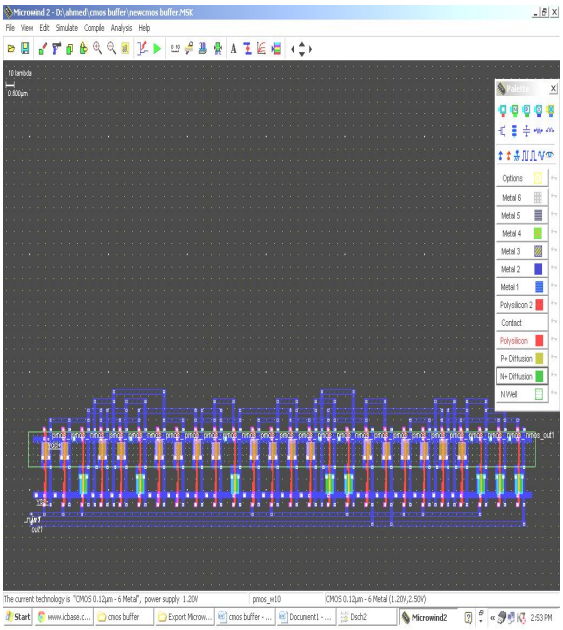
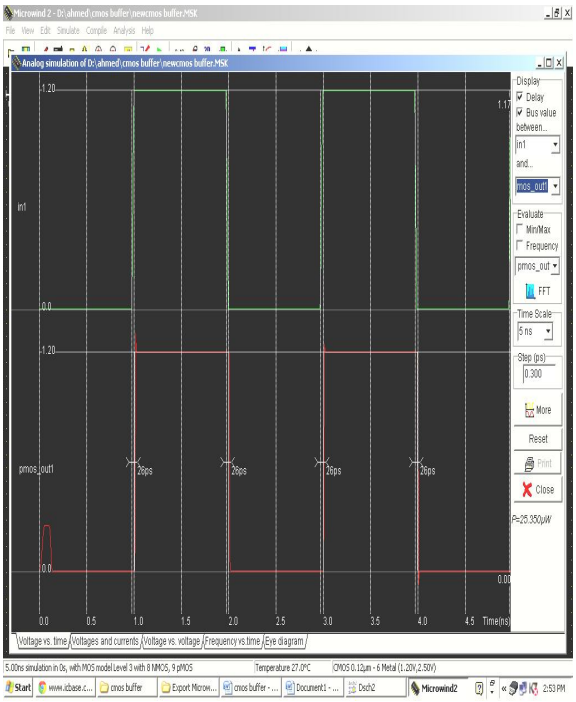
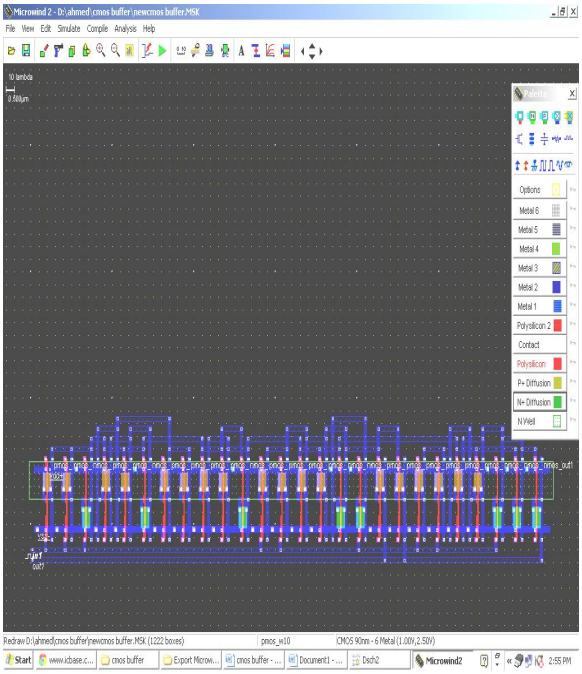
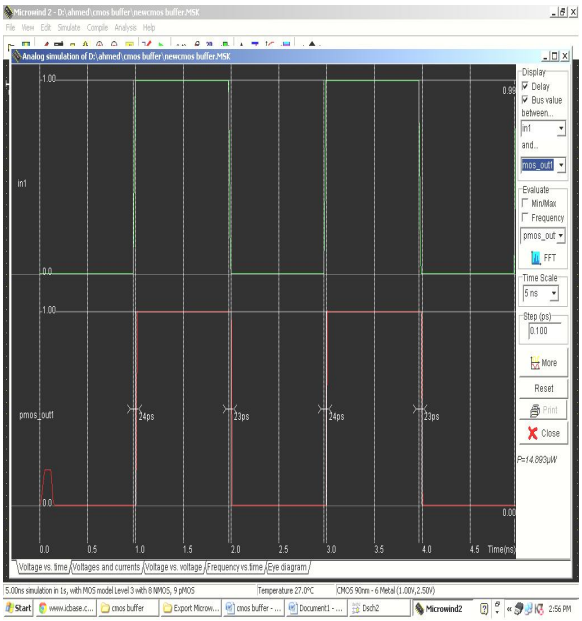
The Layout with 0.12µm technology and analog simulation of enhanced CMOS buffer is shown below





Layout and Analog simulation of 90nm enhanced CMOS buffer is shown below





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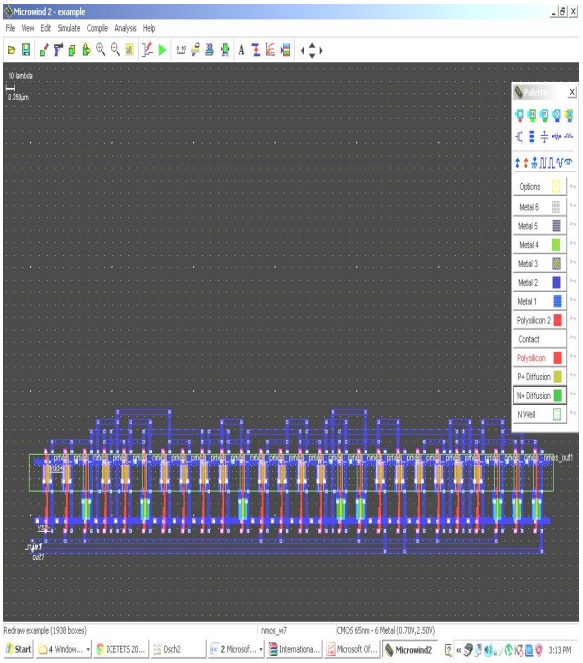
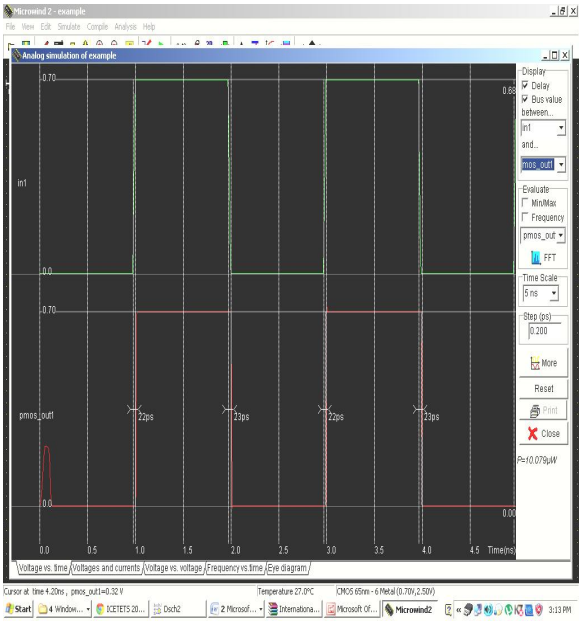
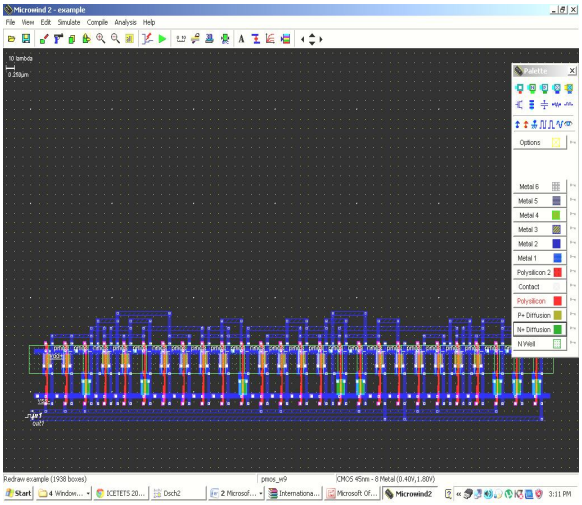
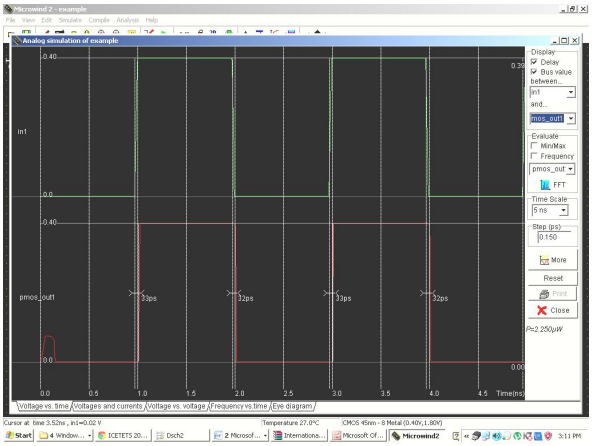
Layout and Analog simulation of Enhanced CMOS buffer with for 65nm technology



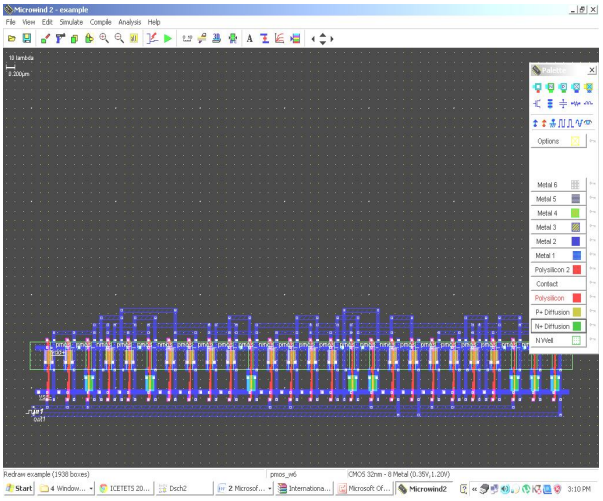


Layout and Analog simulation of Enhanced CMOS buffer with for 45nm technology





Layout and Analog simulation of Enhanced CMOS buffer with for 32nm technology



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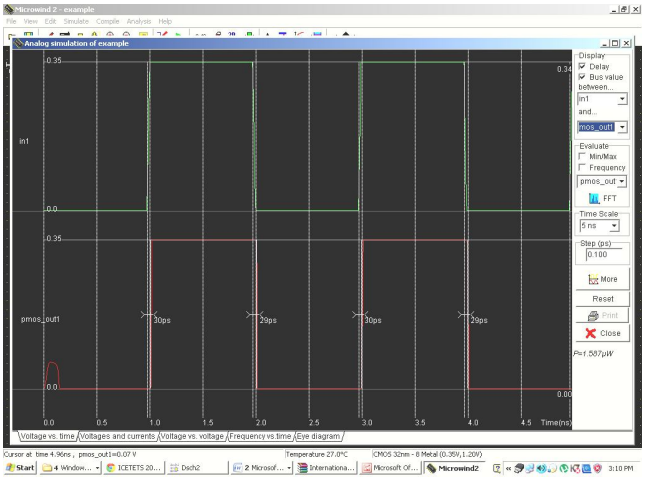

III. RESULTS

Sl.No	Technology	No. of Metals	Power Dissipation
1	0.25µm	6	40µw
2	0.15µm	6	25.35 µw
3	90nm	6	14.89 µw
4	65nm	6	10.079µw
5	45nm	8	2.25 µw
6	32nm	8	1.5 µw

The above result analyses prove that the enhanced CMOS buffer with 32nm technology has lowest power consumption when compared with above various technologies.

IV. FUTURE SCOPE

The novel CMOS Buffer circuits can be designed with inverting and non-inverting modes. Technology below 32nm can be used with degradation of functionality of the CMOS buffer circuit.

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[7] http://www.csus.edu/indiv/p/pangj/274/handout/Handout_Effects%20of%20buffer%20insertion.pdf