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A Low Power Consumption Gilbert-Cell Mixer in 65 nm CMOS Technology

Raja MAHMOU[1], Khalid FAITAH[2]

[1, 2] LGECOS, ENSA Marrakech, Cadi Ayyad University, Morocco
[1] rajae.mahmou@yahoo.fr
[2] k.faitah@uca.ma

ABSTRACT

In this work, we present a design and simulation of low power consumption down conversion Gilbert-Cell mixer, in the 1.9 GHz wireless application. The circuit is in a 65 nm – CMOS technology at a supply voltage of 1.8 V. The obtained results show a third order input intercept point (IIP3) and a Noise Figure in the order of 1.7 dBm and 3.13 dB respectively, when the conversion gain equal to 13.97 dB, and a power consumed equal to 2mW. These performances justify a Low power, Low Noise and an acceptable Linearity of this mixer compared to others approaches found in the literature.

Key words: 65nm technology, Gilbert-cell, noise figure, conversion gain, linearity, power consumption

1. INTRODUCTION

Mixer is an essential block in any telecommunication system which has a critical impact on the performances of all system functions. It is an analog multiplier, as shown in Figure 1 (a), which allows a time multiplication of two signals, for down conversion mixer the first one (RF signal) comes from the receiver antenna after has been filtered and amplified, and the other signal (LO signal) comes from a local oscillator [1].

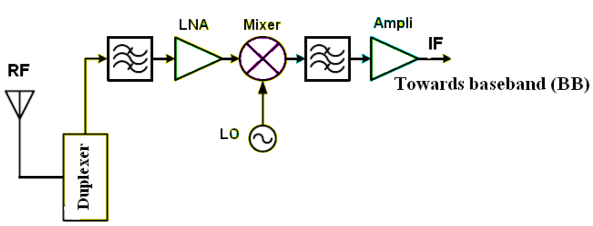

Figure1(a): RF receiver building blocks

The use of CMOS technology to reach a very high levels of integration, offers a significant advantages for the implementation of RF integrated circuits. Indeed, the huge effort made by the microelectronics industry in recent years to reduce the size of transistors, enables the integration of radiofrequency functions with CMOS technology to ever higher frequencies and especially at a very low power levels. It is within this context that the work outlined in this paper. In sum, the goal is not only to design in 65nm CMOS technology an RF Mixer, but also to consider the constraints associated to the nonlinearity, noise and the power consumption of these circuits.

2. MIXER OPERATION

Gilbert Cell is a double balanced mixer, much complex, but have more performance in terms of RF to IF and LO to IF rejection, compared to single balanced mixer: Both LO and RF provide rejection at the IF output, all ports of the mixer are inherently isolated from each other, increased linearity, improved suppression of spurious products than less susceptible to supply voltage noise due to differential topography [2].

As shown in Figure 1(b) the RF signal is applied to the transistors (M2 & M3) which perform a voltage to current conversion. MOSFETs M4 to M7 form a multiplication function, multiplying the linear RF signal current from (M2 & M3) with the LO signal applied across M4 to M7 which provide the switching function. (M2 & M3) provide +/- RF current and (M4 & M7) switch between them to provide the inverted RF signal to the left hand load. (M5 & M7) switch between them for the right hand load. The two load resistors form a current to voltage trans-formation giving differential output IF signals [2].
The principal parameters adopted to characterize RF mixer are: Conversion Gain, Noise Figure, Isolation, Linearity and Power Consumption.

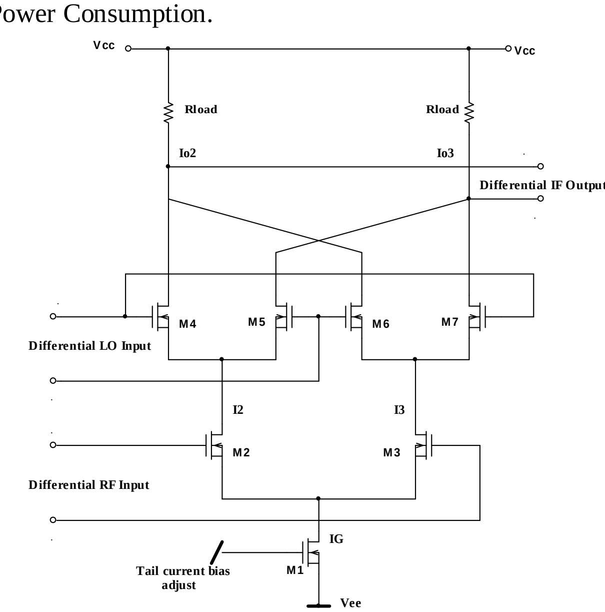

Figure1 (b): Architecture of Gilbert-Cell Mixer

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3. SIMULATION RESULTS

On Agilent ADS tool the Length of MOSFET channel was chosen to maximize gain, to minimize noise and to optimize the footprint of the circuit.

The width of RF input MOSFETs was chosen maximum with respect to current consumption specifications [3]. The bias current of M1 (fig.1.b) is fixed by keeping the bias voltage of CMOS at Vdd = 1.8V, VRF and VLO frequencies are respectively 1.9 and 1.8GHz which provides an intermediate frequency of 100 MHz.

The choice of these values gives an IF frequency as agreed to meet most of the wireless networks deployed today, and operating frequency around 1 GHz, such as GSM [4].

3.1 Transient and harmonics responses

Using ADS tool, the following graphs (figures 2 and 3) show that the proposed circuit realizes the function of mixing frequencies.

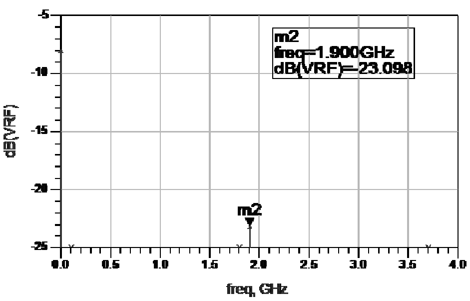

Figure 2: Frequency Input Spectrum at 1.9 GHz

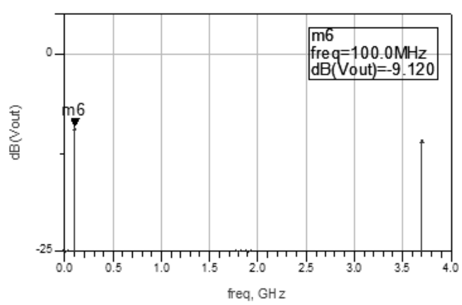

Figure 3: Frequency Output Spectrum

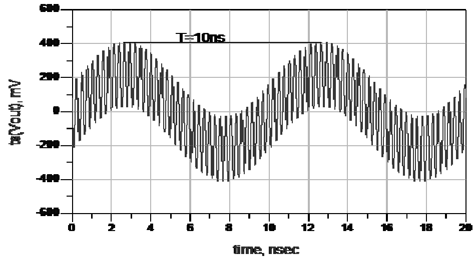

Figure 4: Output signal

The output signals (Figure 4) show a frequency value fRF – fLO equal to about 100 MHz. Other unwanted harmonics are due to the non-linearity of transistors.

3.2. Order 3 Interception Point (IIP3)

The following figure shows an IIP3 value equal to 1.7 dBm.

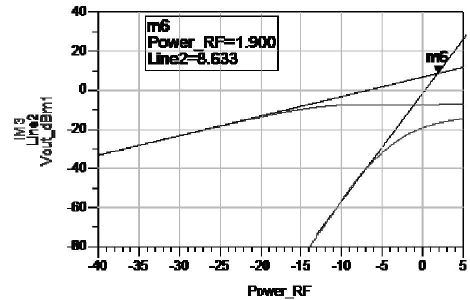

Figure 5: Third Order Input Interception Point (IIP3)

3.3 Noise Figure

Curve noise in the input and in the output, are shown in Figures (6&7):

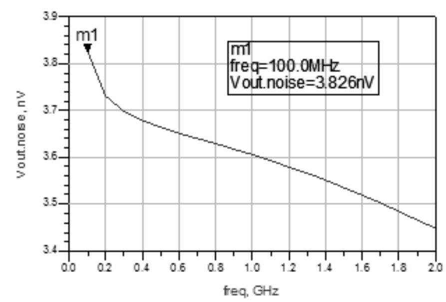

Figure 6: Output **N**oise

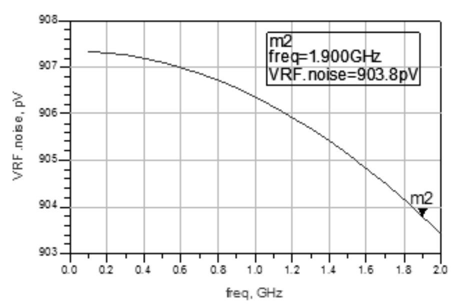

Figure 7: Input Noise

By the relation between Output, Input Noise and the Conversion Gain, the noise figure is equal to 3.13dB.

3.4 Power Consumption

DC simulation, allowed us to measure the power consumption of the mixer circuit which is 2 mW, with Vdd = 1.8V.

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4. PERFORMANCES COMPARISON

We have designed a miniaturized Gilbert-Cell mixer by a 65nm-CMOS technology. Compared to the approaches found in the literature (on Table 1), this circuit presents a very low power consumption, low noise and an acceptable trade between the linearity and gain.

Table 1: comparison of results with recent works

	Proposed Mixer	**[5]**	**[6]**	**Typical Caracteristics [7]**
GC (dB)	**13.97**	9.12	12.42	10
IIP3 (dBm)	**1.7**	10.45	6	5
Power (mW)	**2**	30.78	2	---
NF (dB)	**3.13**	9.74	8.92	12
Technology	**65nm**	0.18um	65nm	**---**
Frequency (GHz)	**1.9**	1.9	1.9	**---**

5. CONCLUSION

The purpose of the presented work is to study the feasibility of a Gilbert Cell in RF chain, dedicated to low power consumption wireless applications; by the 65nm CMOS technology. From the simulation results, the most important parameters characterizing an RF mixer have been measured, that shows the performance of this choice compared to recent technologies.

The obtained results in this study show that the proposed mixer could be used for wireless communication for instance in the WLAN applications.

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