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Transformerless Inverter Topology for Single Phase Application with Elimination of Leakage Current

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ABSTRACT

Various disadvantages such as increased weight, size and cost of single phase photovoltaic converter with transformer has urged the design engineers towards to the transformerless topologies. But, the main challenge of transformer less inverter topology is leakage current. In recent years, many leakage current reduction techniques have been addressed. Many of them are of galvanic isolation. Nevertheless the galvanic isolation can not only results the constant value of common mode voltage (CMV). Hence, it is not possible to achieve complete leakage current elimination. In this work, a transformerless single phase inverter with a clamping method is proposed to obtain constant CMV in all its operating modes. Additionally, a modified modulation approach is also proposed to enable a current path during the negative region of power. Consequently, it is possible to achieve reactive power region by the enabled bidirectional current path in the negative region of power. The result shows the complete clamping of the CMV and reactive power generation by the proposed system. Improved efficiency and reduction of harmonic distortions is also achieved.

Key words: CMV, Leakage current, PV, Power system; Reactive power; SiC, Transformerless Inverter; WBG.

1. INTRODUCTION

It is observed from the literature survey, various topologies of transformerless inverters have been dealt by numerous researches [1, 2, 3, 4]. Main demerit of transformerless inverters is its leakage current flow in absence of transformer. More leakage current flow increases total harmonic distortion (THD), electromagnetic interference (EMI) and thus escalates the overall system losses. In some cases, it may bring about personal safety issues [5]. In many transformerless inverter topologies, the efficiency has been increased by using unipolar modulation technique, thereby reducing the leakage current by truncating the AC side from DC side during the freewheeling operation. This is just the well-known galvanic isolation approach.

Using this approach, various topologies have been introduced inclusive of famous HERIC inverter, H5 inverter and H6 inverter topologies [6, 7]. Since the CMV is unidentifiable by the operating modes, it is very important to note that the galvanic isolation alone cannot mitigate the leakage current. Therefore, modifications are required in modulation techniques and converter topologies as well.

Generally, obtaining unity power factor operation is being the primary objective of modulation techniques. As the grid connected operation of inverters require the reactive power generation as a desirable factor, the bipolar modulation techniques used to generate reactive power increase the switching losses and pull down the efficiency.

From [8, 9], it is found that Si MOSFET based transformerless inverter gives higher efficiency in reactive power generation, but there is a possibility of device failure because of inferior reverse recovery characteristics of Si MOSFET. The main aim of these inverters is to reduce the cost by avoiding complexity due to antiparallel conduction of diode. However, Sic MOSFET yields better performance on its reverse recovery due to shorter life time of its minority carrier [9, 10, 11].

For this reason, SiC MOSFET helps to generate the reactive power neither by modifying the structure of converter nor by increasing the number of freewheeling diodes. Due to the above fact, the wide band gap (WBG) power device, say SiC MOSFET is used in this work in order to offer the reactive power without any structural modification in the converter. Besides, lower THD and higher efficiency is achieved by operating the converter at 100 kHz switching frequency.

2. TOPOLOGY TO ELIMINATE THE LEAKAGE CURRENT

The novel inverter topology introduced in this work is derived from the regular H6 topology where the sixth switch has been

repositioned and connected to the terminal 1. The novel topology and the switching patterns are presented in Figure 1 and 2. Compared to conventional inverter topologies the novel one has low conduction loss, since the number of conducting switches is reduced from six switches to five switches.

Meantime, it is worth to note that galvanic isolation can not only be the solution to maintain a constant value of CMV at the freewheeling process. During the freewheeling, the output terminals 1 and 2 of the inverter would float according to the DC input; hence it is not possible to determine the CMV with the switching processes. Because of this issue, complete control of the leakage current becomes impractical by the galvanic isolation.

Therefore an improved topology as shown in Figure 3 has been implemented using clamping method to obtain invariable CMV at the freewheeling state through which the elimination of leakage current is possible. In order to divide the voltage, the DC link capacitor is divided into two equal halves and connected in series. In the modified structure, an additional switch is inserted between the midpoint of the bifurcated capacitors and the middle of the freewheeling switches.

Since the available modulation techniques are not meant for freewheeling operation in negative region, the inverter cannot generate the reactive power [12, 13, 14]. However, the unipolar PWM can be applied in the negative power region only if the line voltage V_{12} has three voltage ranges such as $+V_{dc}$, $-V_{dc}$ and zero voltage.

Even then, the observation shows that the negative power region cannot attain zero voltage state in absence of current path. Hence, a modified modulation technique is applied as given in Figure 4 to eliminate the leakage current and to generate the reactive power [15].

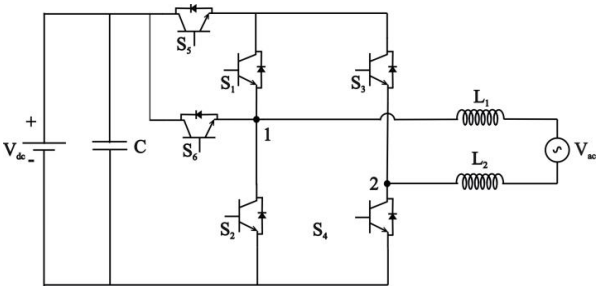

Figure 1: Circuit Diagram of the proposed transformerless inverter topology

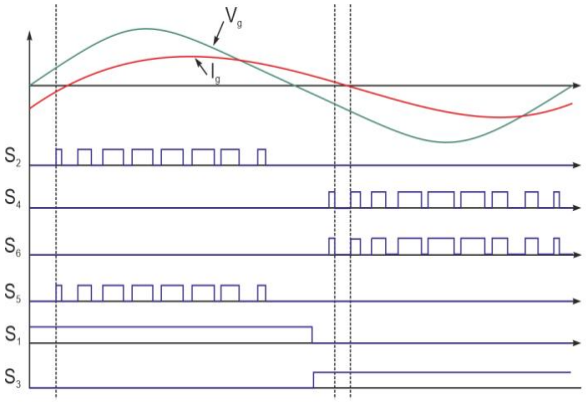

Figure 2: Modulation strategy of the proposed transformerless inverter

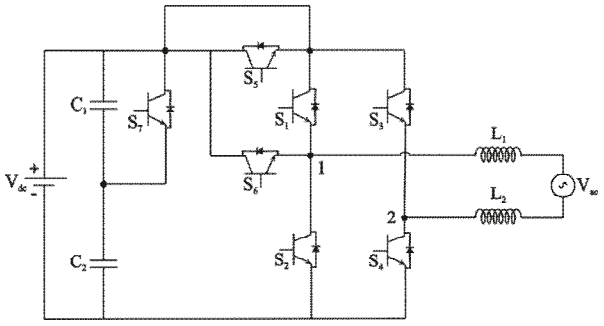

Figure 3: Modified transformerless inverter

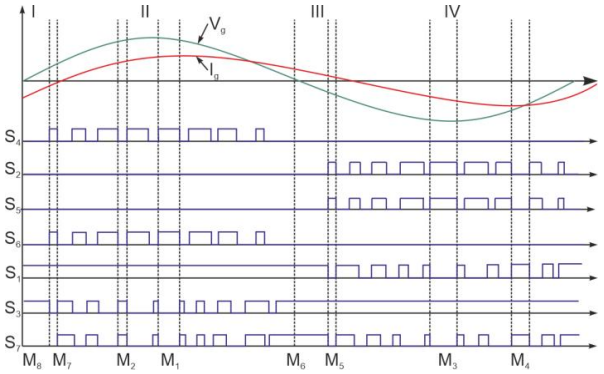

Figure 4: Modified modulation technique

The generation of reactive power cannot be skilled in single-phase transformerless inverter topologies because the existing modulation techniques are not adopted for a freewheeling path in the negative power region [16]. During negative power region, the line to line voltage (V_{12}) must have three values, $+V_{dc}$, $-V_{dc}$, and zero [17]. It is notice that zero voltage states cannot be achieved in the negative power regions because there is no current path established, as illustrated in Figure 4. This modulation method is modified to eliminate the leakage current and to obtain reactive power generation, as shown in Figure 4.

3. MODULATION TECHNIQUE FOR REACTIVE POWER GENERATION

The modulation implemented in this work has 8 modes of operation under 4 regions. Polarity of the current and the voltage determines the power flow in these regions. The power is positive when they are in same polarity and negative when they are in opposite polarity. In the regions 2 and 4, the power flow is positive and it negative in the regions 1 and 3. The Table 1 gives the switching conditions of each mode of operation.

Table 1: Modes of Operation

Mode	Operation	Power Region	Common Voltage
1	Active Mode	Positive	$V_{10}= V_{dc}$ and $V_{20}= 0$ $V_{cm}=\frac{V_{10}+V_{20}}{2}=\frac{1}{2}V_{dc}$
2	Free wheeling Mode	Positive	$V_{10}=V_{20}=\frac{1}{2}V_{dc}$ $V_{cm}=\frac{V_{10}+V_{20}}{2}=\frac{1}{2}V_{dc}$
3	Active Mode	Positive	$V_{10}=0$ and $V_{20}=V_{dc}$ $V_{cm}=\frac{V_{10}+V_{20}}{2}=\frac{1}{2}V_{dc}$
4	Free wheeling Mode	Positive	$V_{10}=V_{20}=\frac{1}{2}V_{dc}$ $V_{cm}=\frac{V_{10}+V_{20}}{2}=\frac{1}{2}V_{dc}$
5	Active Mode	Negative	$V_{10}=0$ and $V_{20}=V_{dc}$ $V_{dm}=V_{12}=-V_{dc}$ $V_{cm}=\frac{V_{10}+V_{20}}{2}=\frac{1}{2}V_{dc}$
6	Free wheeling Mode	Negative	$V_{10}=V_{20}=\frac{1}{2}V_{dc}$ $V_{dm}=V_{12}=0$ $V_{cm}=\frac{V_{10}+V_{20}}{2}=\frac{1}{2}V_{dc}$
7	Active Mode	Negative	$V_{10}=V_{dc}$ and $V_{20}=0$ $V_{cm}=\frac{V_{10}+V_{20}}{2}=\frac{1}{2}V_{dc}$
8	Free wheeling Mode	Negative	$V_{10}=V_{20}=\frac{1}{2}V_{dc}$ $V_{dm}=V_{12}=0$ $V_{cm}=\frac{V_{10}+V_{20}}{2}=\frac{1}{2}V_{dc}$

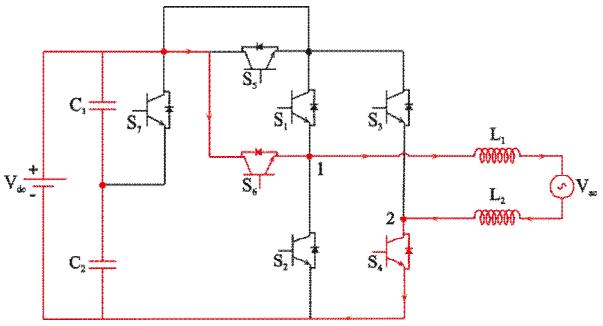

Figure 5: Current path during Mode 1

Mode 1: The switches S_1, S_6 and S_4 are switched ON and the remaining switches are in OFF condition. The current flows through the switches S_6 and S_4. But the switch S_1 doesn't carry any current and hence offers no conduction loss(figure 5).

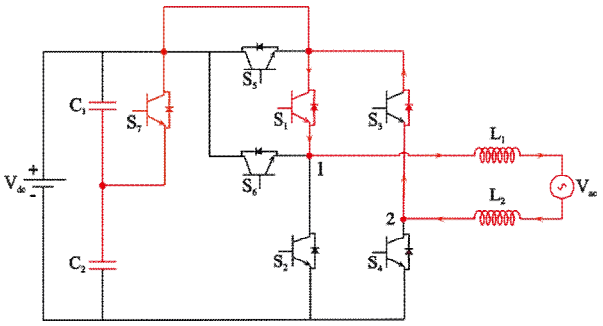

Figure 6: Current path during Mode 2

Mode 2: The switches S_1, S_3, and S_7 are switched ON and other switches are switched OFF. The current flows through the path established by the switch S_1 and the diode of switch S_3(figure 6).

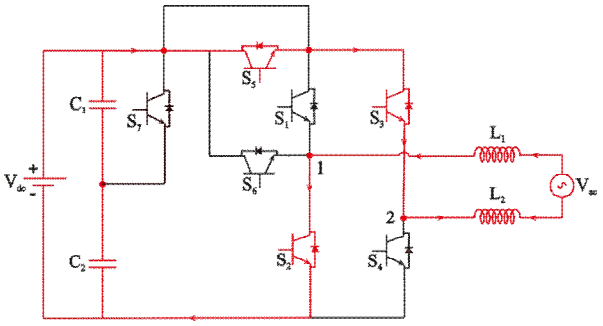

Figure 7: Current path during Mode 3

Mode 3: The switches S_2, S_3 and S_5 are switched ON and carry the current whereas other switches are kept OFF (figure 7).

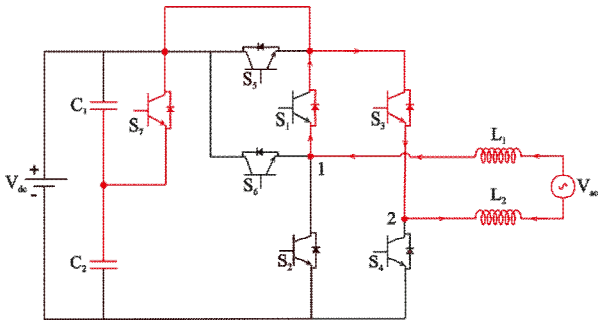

Figure 8: Current path during Mode 4

Mode 4: The switches S_1, S_3 and S_7 are switched ON and other switches are kept OFF. The current flows through the switch S_3 and the diode of S_1 (figure 8).

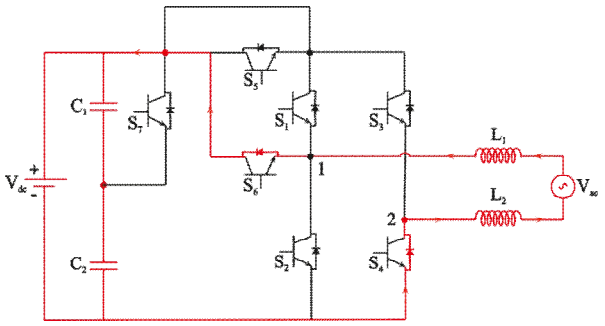

Figure 9: Current path during Mode 5

Mode 5: The switches S_2, S_3 and S_5 are switched ON and the remaining switches are kept OFF. The freewheeling current flows through the diodes of switches S_2, S_3 and S_5 (figure 9).

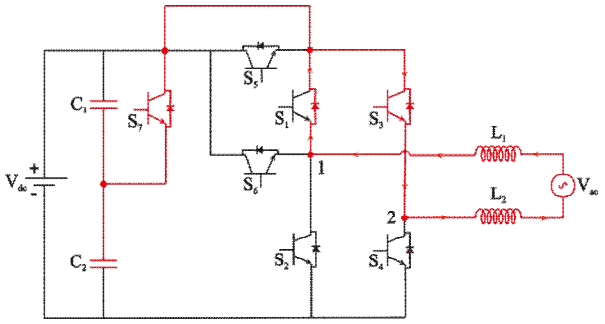

Figure 10: Current path during Mode 6

Mode 6: The switches S_1, S_3 and S_7 are switched ON in this mode whereas other switches are kept OFF. The current flows through the switch S_1, and the diode of the switch S_3 (figure 10).

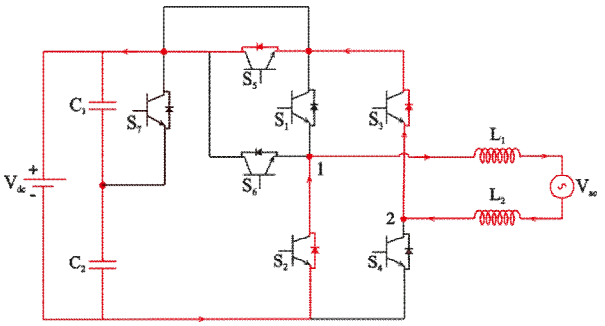

Figure 11: Current path during Mode 7

Mode 7: The switches S_1, S_4 and S_6 are switched ON and the other switches are kept OFF. During this period, freewheeling action is taken by the diodes of the switches S_4 and S_6 (figure 11).

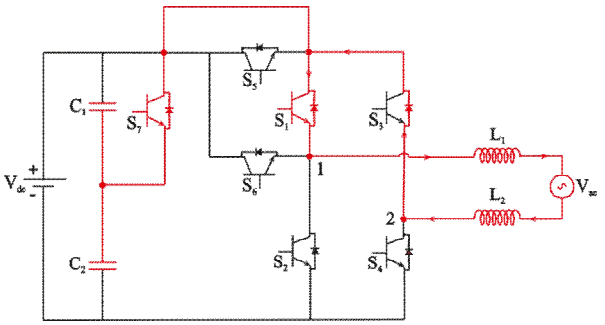

Figure 12: Current path during Mode 8

Mode 8: The switches S1, S3 and S7 are switched ON in this mode and other switches are kept OFF. The current is thus flows through S3 and the diode of the switch S1. This switching state generates zero voltage condition (figure 12). The modified modulation technique helps to obtain the zero voltage so that the output contains $+V_{dc}$, $-V_{dc}$ and zero voltage state. Consequently, the modulation provides the bidirectional flow of current during negative region of power and thus offers reactive power.

4. RESULTS AND DISCUSSION

This research work is used MATLAB/SIMULINK software to design the proposed topology and to evaluate its performance. The circuit parameters of the designed system design are given in Table 2. The simulation was carried out in the switching frequency of 10 kHz.

Table 2: Design parameters of the inverter topology

Parameters	**Rating**
Input Voltage	800 V
Grid Voltage	230 V
Supply Frequency	50 Hz
Switching Frequency	10 kHz
DC Bus Capacitance	950 µF
Parameters	**Rating**
Parasitic Stray Capacitance	350 nF
Output Power	3 kW

It is observed that the voltage waveform of V_{10} and V_{20} are of oscillating nature. Furthermore, the common mode voltage V_{cm} is also oscillating and not being constant at 400V. This causes a leakage current flow that cannot be eliminated. To deal with this problem, the novel topology is thus modified by incorporating a clamping method. The respective common-mode characteristics, viz, V_{10}, V_{20}, V_{cm} and the leakage current are shown in Figure 13 in which the voltage waveforms of V_{10} and V_{20} are almost smooth and complementary. Because of this, the V_{cm} is clamped to a constant 400V throughout the operating period and leakage current elimination is achieved.

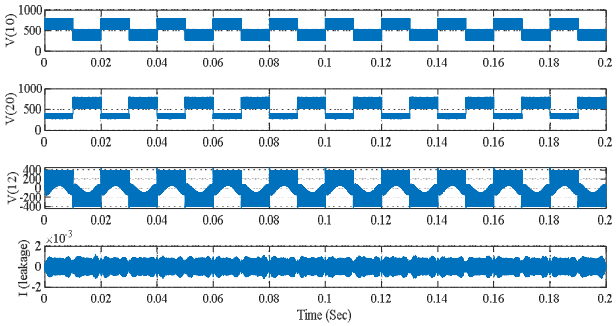

Figure 13: Common mode (CM) characteristics of the proposed topology

It is observed that the introduced modified topology performed well in handling the reactive power with lower harmonic distortion at the rate of 3.15% which is very lesser than that yielded by the conventional modulation techniques.

5. CONCLUSION

The stray capacitances established by the inverter circuit is charged and discharged by the common-mode voltage according to the switching frequency. Therefore, formation of a resonant circuit is possible by the stray capacitor, impedance of the grid and filter circuit inductances. Due to the formation of a resonant circuit, leakage current will flow through the parasitic components of the circuit. This leakage current results more system loss, higher distortions, interference issues and some safety issues. In this work, a modified inverter topology with an additional switch is proposed to obtain a constant CMV and to eliminate the leakage current. It also provides a current path at zero voltage state for reactive power generation with the modulation technique implemented.

6. FUTURE SCOPE

The electromagnetic interference (EMI) effect of the leakage current passing through the system can be analyzed in future work. During implementation in larger scale power generation in PV applications, the impact of EMI will be a greater concern.

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