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Design of Novel Low Power 6T XNOR based Full Adder and Full Subtractor and Comparison of Various Adders and Subtractors

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ABSTRACT

Portable high speed digital devices are an emerging area and the designing of such circuits in VLSI is the need of the hour. Arithmetic and logic functions are the main blocks of such designs. Adders and subtractors are used in complex data processing to perform arithmetic operations. Designing of adders and subtractor using 6T XNOR demonstrates Low power, high speed switching and also optimized Area by means of transistor count compared to conventional adders and subtractors. This paper presents novel approach for 6T XNOR based full adder and full subtractor circuits. The circuit realization has been performed using DSCH and waveforms are obtained by using Micro wind 3.1

Key words: DSCH, Full Adder, Full Subtractor, Low Power, Micro wind 3.1, VLSI, 6T XNOR.

1. INTRODUCTION

In many of the VLSI application we see the significant use of arithmetic operations. Most of the arithmetic and logic applications requires adders and subtractors as their primary component. Circuit realization for low area and power has become an important issue with the growth of integrated circuit. Minimum power and Minimum time delay are the main functions to design the logic for the VLSI Circuits. Minimizing the transistor in the design of full adders and full subtractors which forms the basic building blocks of all digital VLSI circuits has been undergoing to, minimizing the power consumption and increasing the speed Owing to the significant role that XNOR gates play in a variety of circuits, particularly arithmetic circuits, optimal XNOR circuit design is required to achieve low size and latency. The primary concern to design XNOR gate is to obtain low power consumption, delay and full output with low number of transistors to implement it.
To improve various circuits, designers use different logic design techniques such as complementary MOS (CMOS), and pass transistor logic, GDI. Each of these methods has a unique design mechanism, along with some benefits and drawbacks. As we know that there are conventional CMOS are the traditional work horse for building digital circuits. The conventional adder uses different number of transistors to design Full adders and Full subtractors like 28T,16T,14T,10T,8T etc... are used for the implementation by using CMOS technique. Full adders and Full subtractors which has the least number of transistors has described to be the best design to achieve low power consumption. Reducing transistor count is a powerful technique for lowering power consumption in circuits. PTL and GDI both use fewer transistors compared to standard CMOS designs for adders and subtractors, this reduction in transistors leads to lower power consumption and known to increase the efficiency of area. Previous circuits are summarized and compared with our new approach.

2.EXISTING METHOD

2.1 14T Full Adder and Full Subtractor

The Full Adder and Full Subtractor are designed using 14transistors. Here the circuits are implemented using XOR and XNOR and Multiplexer logic and these are designed using
CMOS logic [5]. The schematic of 14T Full Adder and Full Subtractor are shown in Figure 1, Figure 2.

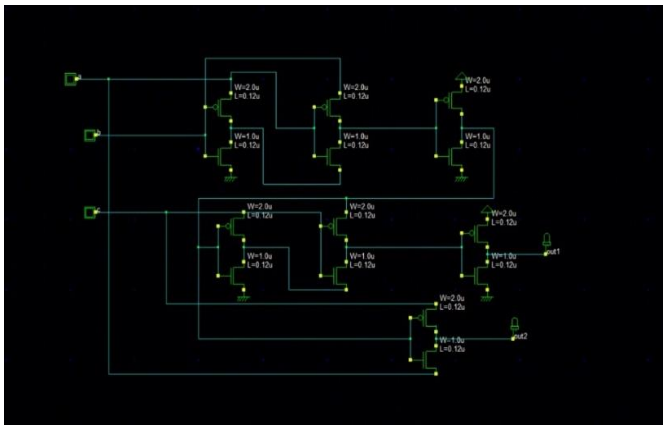

Figure 1: 14T Full Adder

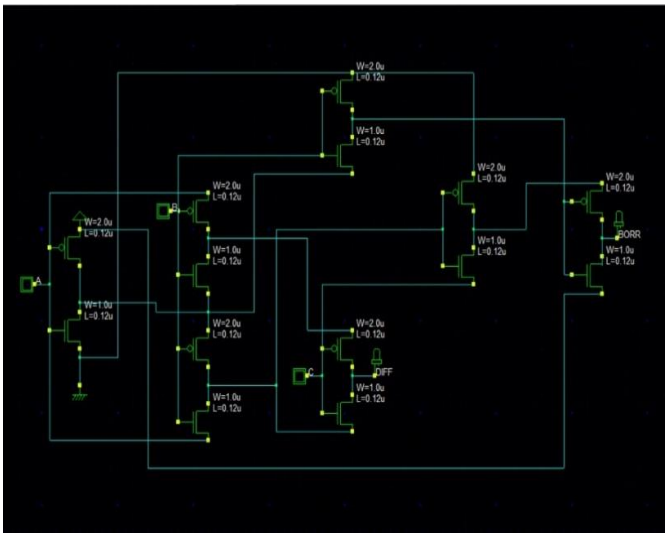

Figure 2: 14T Full Subtractor

2.2 10T XOR based Full Adder and Full Subtractor

In these circuits XOR circuits are used as major component for designing the full adder. In previous design the Full adder and Full Subtractor is designed by using 14 transistors, which can dissipate more power compare to this work [2].

The XOR based 10T Full adder and Full Subtractor is shown in Figure 2, Figure 3. This 10-transistor Full adder and Full Subtractor are implemented using two 4T XOR gates and 2T mux with GDI.

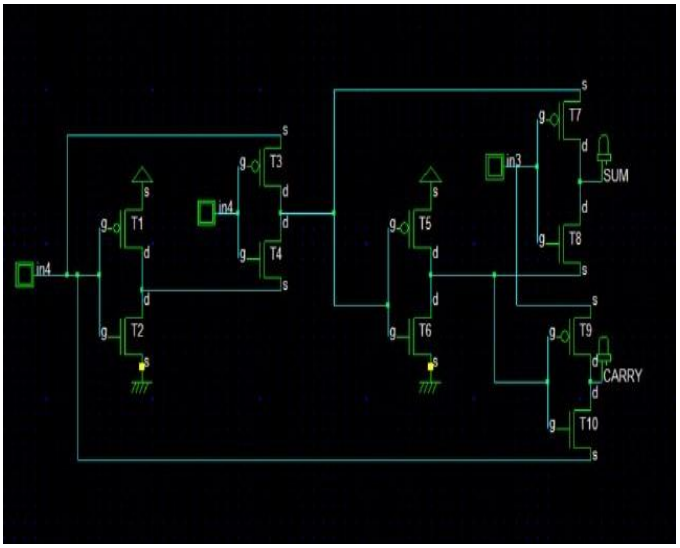

Figure 3: 10-T XOR Based Full Adder

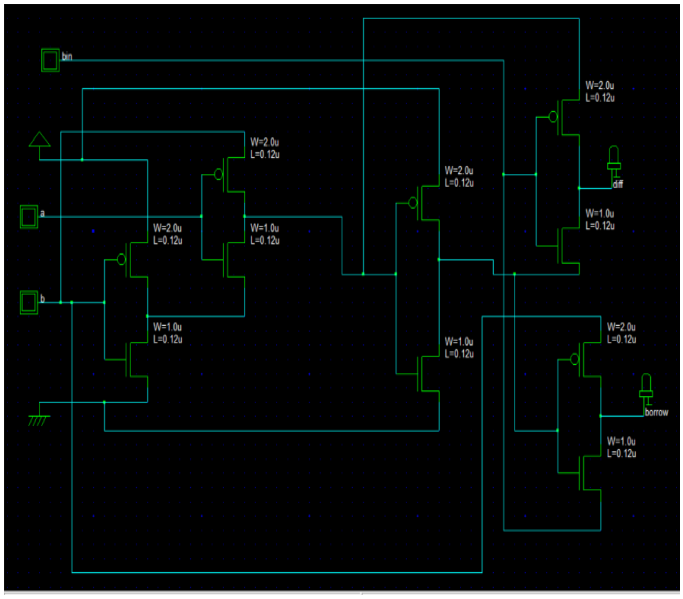

Figure 4: 10-T XOR based Full Subtractor

2.3 10T XNOR based Full Adder and Full Subtractor

The Full Adder and Full Subtractor is designed using XNOR and Multiplexer Modules. This Circuits are designed Using GDI Technique [2]. The XNOR based 10T Full Adder and Full Subtractor are implemented using two 4T XNOR gates and 2T mux, which can reduce power dissipation compared to previous circuits. The Schematics of these Circuits are shown in Figure 5, Figure 6.

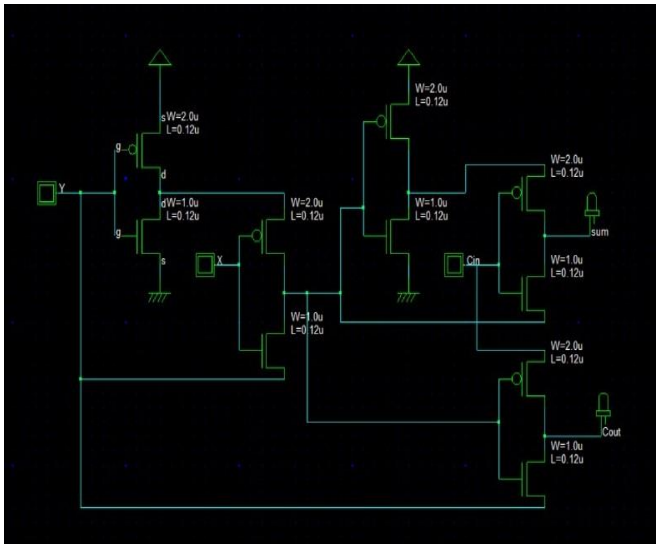

Figure 5: XNOR based 10T FULL ADDER

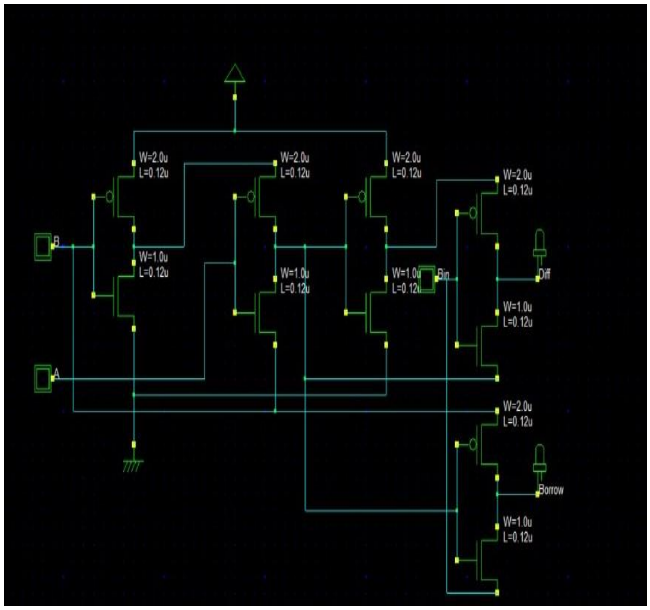

Figure 6: XNOR based 10T Full Subtractor

2.4 8T Full Adder and Full Subtractor

The Design of 8T Full Adder and Full Subtractor are implemented using XOR and Multiplexer Modules [3]. These circuits are designed Using GDI technique. Here we use two 3T XOR and 2T mux to design 8T Full adder and Full Subtractor [4]. The Schematic of XOR based 8T Full Adder and XOR based 8T Full Subtractor are Shown in Figure 7, Figure 8.

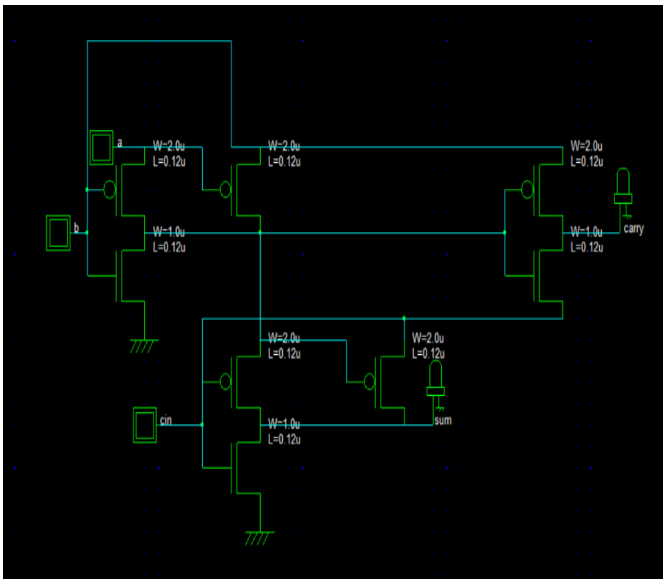

Figure 7: 8T Full Adder

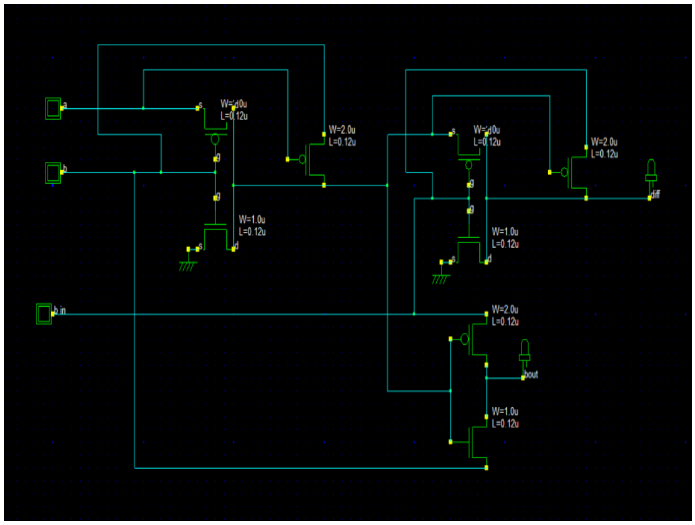

Figure 8: 8T Full Subtractor

3.PROPOSED METHOD

3.1 XNOR based 6T FULL ADDER

The new design of full adders which forms the basic building blocks of all digital VLSI circuits has been undergoing a considerable improvement, being motivated by three basic design features, viz. minimizing the transistor count, minimizing the power consumption and increasing the speed. This paper presents 6T XNOR based Full adder using two transistors XOR gates and one two transistor MUX implemented.

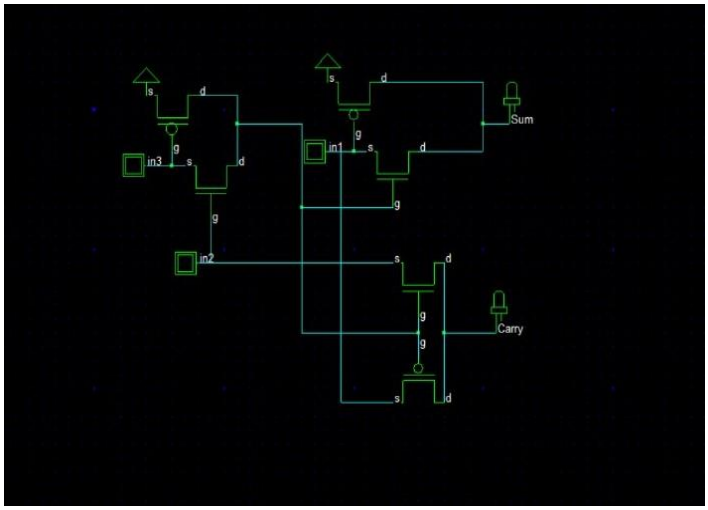

Figure 9: XNOR based 6T Full Adder

The Realization of the 6T XNOR based Full Adder is the Input A is connected to the gate of TI and source of T2. Input B is connected to the gate of T2 and to the source of T5. Input C is connected to the gate of T3 and to the source of T4, T6. The Output of First XNOR i.e. the common drain terminal of T1 and T2 is connected to the common gate terminal of T5 and T6 and also connected to the gate of T4. The VDD is given to source terminal of T1, T3. The output SUM is taken from second XNOR i.e. common drain terminal of T4 and T5. The output CARRY is taken from common drain terminal of MUX i.e. T5 and T6.

3.2 6T XNOR based FULL SUBTRACTOR

The new design of 6T XNOR based Full Subtractor is implemented using two 2T XNOR and one 2T MUX to decrease the transistor count, low power consumption and high speed.

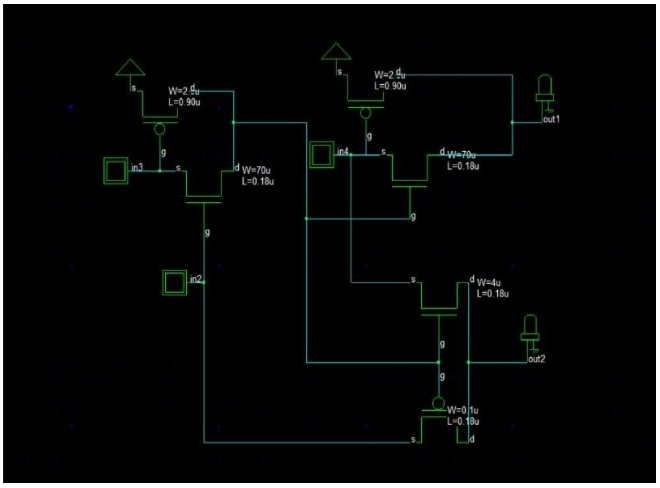

Figure 10: XNOR based 6T Full Subtractor

The realization of 6T Full Subtractor is the Input A is connected to the gate of TI and source of T2. Input B is connected to the gate of T2 and to the source of T6. Input C is connected to the gate of T3 and to the source of T4, T5. The Output of First XNOR i.e. the common drain terminal of T1 and T2 is connected to the common gate terminal of T5 and T6 and also connected to the gate of T4. The VDD is given to source terminal of T1, T3. The output SUM is taken from second XNOR i.e. common drain terminal of T4 and T5. The output CARRY is taken from common drain terminal of MUX i.e. T5 and T6.

4.RESULT

The simulation has been carried out using DSCH 3.1, starting from transistor-level design and further verified using Micro wind 3.1environment. The Simulation Result of XNOR based 10T Full Adder and Full Subtractor is shown in Figure 11, Figure 12.

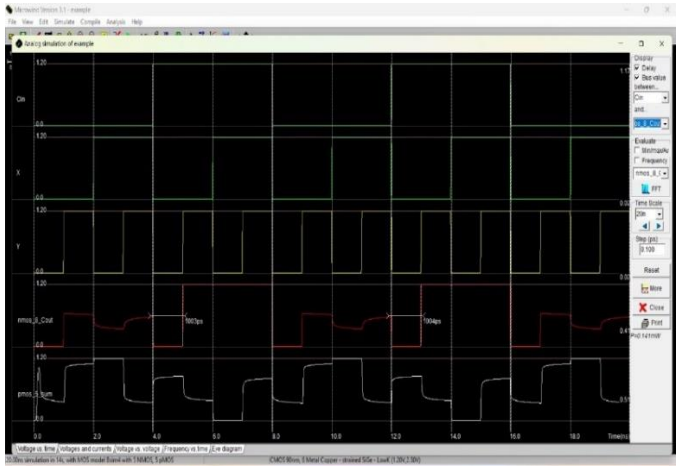

Figure 11: Simulation of XNOR based 10T Full Adder

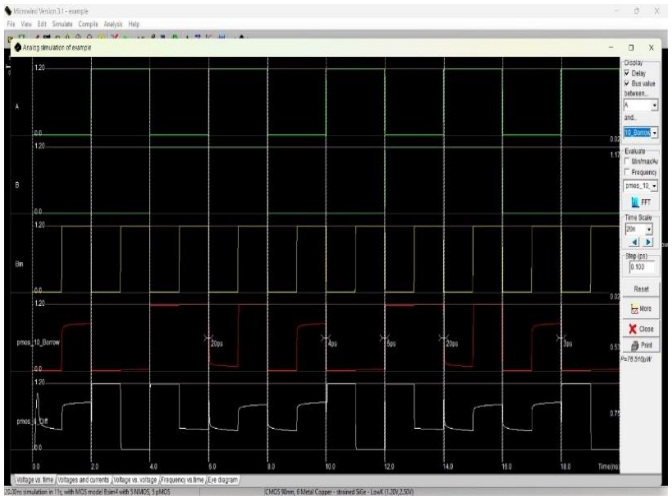

Figure 12: Simulation of XNOR based 10T Full Subtractor

The proposed 6T XNOR based Full adder and Full Subtractors by using two 2T XNOR and 2T MUX are simulated using Micro wind 3.1. All the results are obtained in 90nm CMOS process technology. The Simulation of XNOR based 6T Full Adder is shown in FIG.11 and the Simulation of XNOR based 6T Full Subtractor is shown in Figure 12.

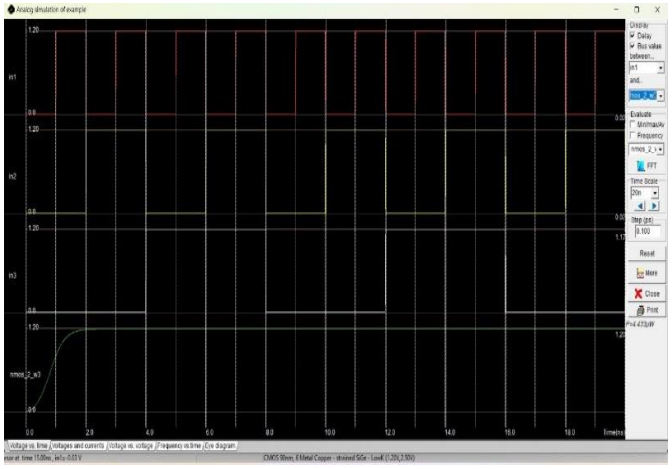

Figure 13: Simulation of 6T Full Adder

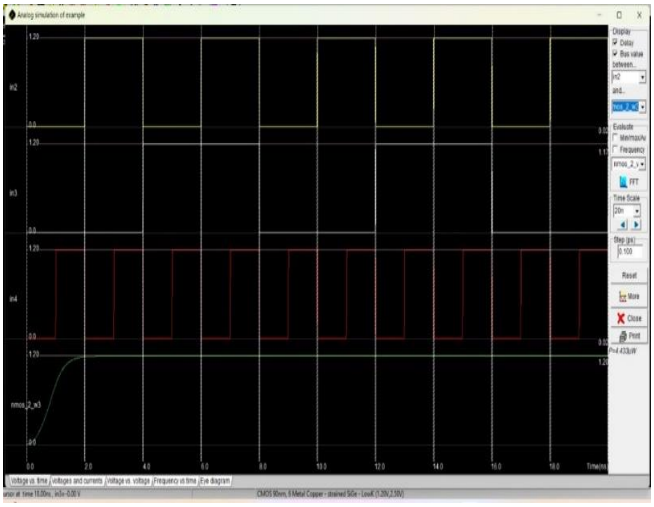

Figure 14: Simulation of 6T Full Subtractor

Table 1 shows the comparison of various parameters of different techniques used for full Adder and Full Subtractor design. We have made our comparison on basis of power consumption and area occupied on a chip based on transistor count. Some graphical analysis has been carried with the help of this table that is shown in Figure 15.

Graphical Analysis shows the comparison of Power Consumed and Area based on Transistor Count for XNOR based 6T Full adder and Full Subtractor with previous design of XNOR based 10T Full Adder and Full Subtractor.

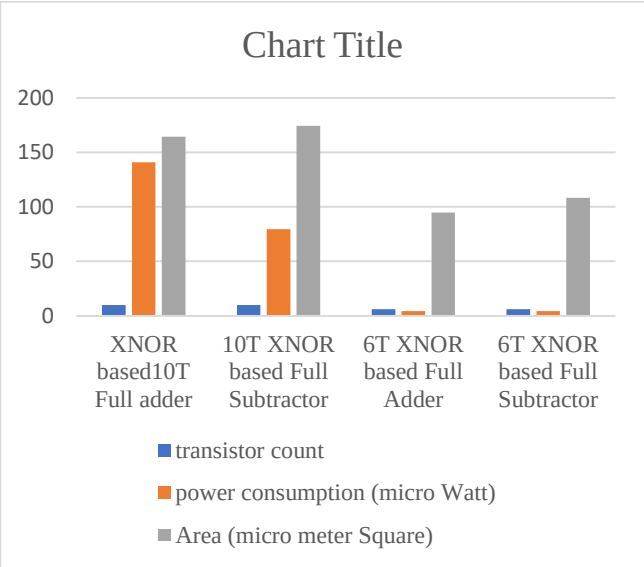

Figure 15: Graphical Analysis

Table 1: Result summary based on transistor count, area on chip, and average power

PARAMETERS	10T XNOR based Full Adder	10T XNOR based Full Subtractor	6T XNOR based Full Adder	6T XNOR based Full Subtractor
Number of Transistor Required	10	10	6	6
Power Consumed (micro-Watt)	141	78.510	4.33	4.433
Area on Chip(um^2)	164.3	174.3	94.9	108.3

5.CONCLUSION

In this paper, we proposed the design of XNOR based Full Adder and Full Subtractor circuit using only 6 transistors. The performances of this circuit have been compared based on parameters like areas and power with earlier designed XNOR based 10T Full Adder and Full Subtractor. The proposed design of a 6T full adder and Full Subtractor uses a novel 2T XNOR gate. Since Transistors are directly proportional to area and power, we have achieved drastically low power adder and subtractor due to the modified design based on only six Transistors.

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