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Design of Low Noise Low Power Instrumentation Amplifier for Biomedical Applications

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ABSTRACT

Advancements in integrated circuit (IC) technology and circuit design are enabling devices to replace complex biological applications. Despite this progress, achieving necessary functionality at low power levels is crucial for fully integrated systems. Biomedical devices like pacemakers, which require ongoing battery charging, operate at nanowatt power levels over several years. To ensure long-term pacemaker survival, an Analog Front End (AFE) with low to moderate power consumption and high precision is essential. The front-end Instrumentation Amplifier (INA) is vital for signal acquisition, significantly improving the effectiveness of ECG signal collection systems.The primary aim of this research is to develop an integrated ECG instrumentation amplifier (INA) that can deliver top-notch performance while keeping noise and power consumption to a minimum. This amplifier will enable seamless monitoring of the ECG signal without interruptions. Using an AC connected Common Mode Feedback system [1]. in conjunction with an Operational Trans-conductance Amplifier (OTA) that uses a Chopper stabilization technique, the study's band pass filtering response within the ECG signal frequency range of 0-100Hz is obtained as anticipated. CMOS 45 nm technology is used throughout the entire process using Mentor Graphics EDA Tools.

Key words: Analogue Front End, Instrumentation Amplifier, Operational Trans-conductance Amplifier, CMOS, EDA tools, ECG, Common Mode Feedback System.

1. INTRODUCTION

Medical electronics has improved to the point that extraordinary healthcare facilities are now possible thanks to developments in integrated circuits, microelectronics, material technologies, and micro-mechanics. Clinical professionals can identify and cure illnesses with the help of these dependable, technologically intelligent, and integrated devices.

They are driving the wellness revolution by shifting from traditional sickness-oriented equipment to prevention-oriented medical devices. Health care application systems and implantable medical devices have become key components of this revolution as shown in Figure 1. Miniaturization, intelligence, and informationization have been made possible by developments in medical electronics and integrated circuit technology. Individuals can now easily control and analyze medical devices and healthcare systems, enabling them to be wirelessly connected to the internet and other networks.

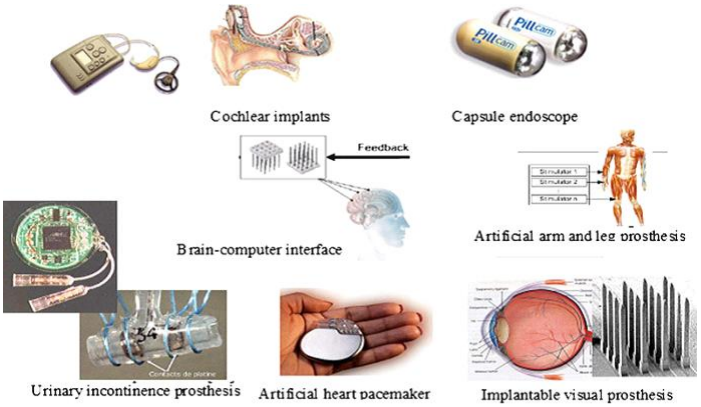

Figure 1: Symbolizes cutting-edge medical equipment

Modern advancements in CMOS technology are driving the expansion of implanted medical devices and healthcare equipment. CMOS-based integrated circuits [2]. are known for low power consumption, good noise tolerance, and strong scaling down characteristics, following Moore's law to increase complexity and speed while lowering costs.

1.1 Implantable Devices

Devices intended for surgical implantation into the human body and prolonged bodily retention are referred to as implants. Based on how they get electricity, implantable devices can be classified as either passive or active. Implants classified as passive do not require a power source to transfer energy to the human body, whereas active implants do. One such example is a metallic bone prosthetic. The Active Implantable Device [3]. in this application has to be powered by batteries. For extended usage of these devices, it is necessary to surgically replace the batteries, which guarantees the need to minimize power consumption. In rare instances, the system is driven by radiofrequency radiation emanating from sources external to the body. Nevertheless, this isn't always feasible, and there are still significant issues with its utilization.

1.There are several functions that an implanted electronic device can carry out. The following are the main roles:

The patient or the consulting physician is given access to certain physiological parameters that have been measured. These professions fall under the category of "telemetry," in which "metry" denotes calculation and "tele" denotes distance. Either the patient or the doctor may oversee the entire process of remotely monitoring physiological data from outside the body.

2.Applying the appropriate level of electrical stimulation, as determined by discussion or consultation with the doctor. In this scenario, using a switch outside the body is advised by the doctor.

1.2 Impantable Cardiac Pacemakers

Due to its extensive use, the cardiac pacemaker is the most successful example of a cardiac implanted device. An artificial pacemaker is necessary to speed up the patient's heartbeat when it beats too slowly, which is unnatural for the human heart. This pacemaker [4]. facilitates the heart's return to a steady heart rate. Thus, the body receives the necessary amount of blood. An electrical stimulator that resembles an artificial cardiac pacemaker is depicted in Figure 2. After that, the patient's chest skin is punctured just below the collar bone to implant the cardiac stimulator. The electrodes attached to the heart receive continuous electrical pulses created and sent by the pacemaker. The outermost layer of the heart walls, called the epicardium, is where these electrodes are firmly positioned.

The cardiac implantable device stimulates the heart muscle in a rhythmic and controlled manner. As a result, the heart pumps as it normally would.

For prosthesis users whose hearts don't beat or pound at the appropriate rate, this result may be helpful. Thus, pacemakers can be thought of as cardiac rhythm controllers that can handle intricate cardiac disorders. A typical cardiac pacemaker's primary goal is to continuously monitor and evaluate a patient's heart rhythm in order to detect any irregularities. Electrical pulses are used to control and stimulate the heart if any aberrations are found. Moreover, an artificial pacemaker is, by definition, a real-time automated electronics system. It has the hardware and software components required for effective operation. An electrical power source, typically a battery, an electrode unit with leads electrically connecting the pulse generator and heart, and an electrical pulse generator are the three main parts of a cardiac pacemaker. As shown in Figure 3, The electrical connections between the human heart and the pulse generator.

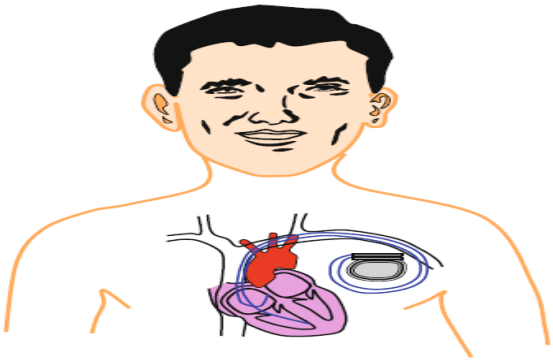

Figure 2: Individual having a pacemaker implanted

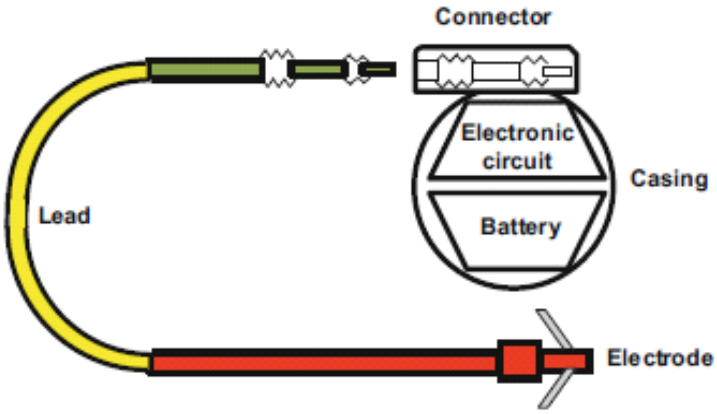

Figure 3: External view of a cardiac pacemaker demonstrating the electrical connection between electrodes and a pulse generator

1.3 Problem Statement

Health care devices that run on batteries, especially implanted ones, should incorporate several functionalities such as digital signal processing and biomedical data gathering. These devices are often powered by tiny batteries. As a result, there are analog and digital components in the CMOS device. Additionally, the CMOS technology has the ability to scale down, which results in a smaller device area. Compared to digital circuitry, the design of analog circuitry is more complex due to space and power limitations.

The implanted ECG signal acquisition system remains unaffected. However, cardiovascular pacemakers necessitate surgical replacement every five to seven years due to battery limitations. To extend pacemaker lifespan, it's crucial to develop an Analog Front End (AFE) with low power consumption, high accuracy, and moderate speed. The AFE's front-end Instrumentation Amplifier (INA) plays a pivotal role, as the quality of the signal it generates directly impacts the reliability of the ECG signal gathering system .

Ensuring low-power dynamic comparator design is essential for maintaining ADC performance within specified limits. Factors such as kickback noise, offset parameters, and leakage currents can significantly impact an ADC's output quality. In the context of cardiac pacemakers, Figure 4 illustrates the different power-usage blocks.

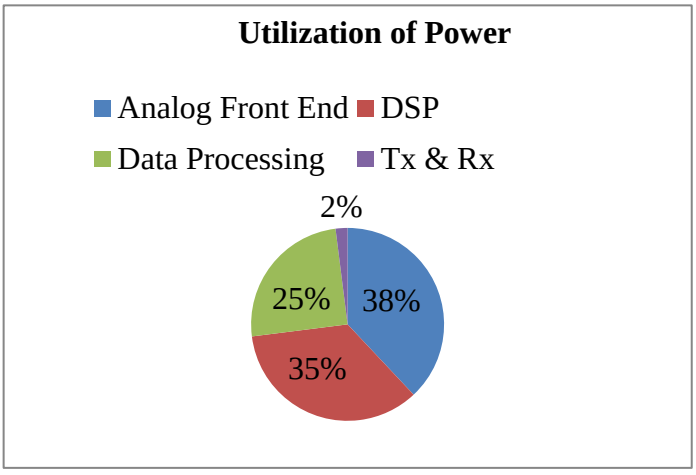

Figure 4: Power use of different Pacemaker blocks

The Analog Front End (AFE) in a pacemaker plays a crucial role. It includes an Instrumentation Amplifier (INA or IA) for receiving cardiac signals and a SAR-ADC [5]. to convert analog inputs into digital data. Notably, the AFE

consumes most of the pacemaker's power. After digitization, a digital signal processor processes the data. While data transmission and reception require minimal power, internal data processing within the pacemaker is energy-intensive. Refer to Figure 5 for the AFE's block diagram.

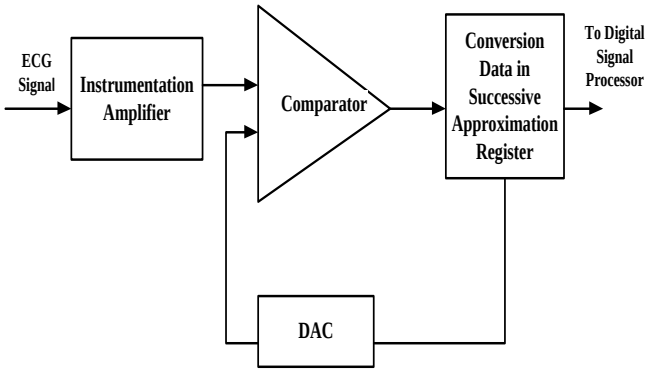

Figure 5: Block schematic of the Analog Front End (AFE) used in the acquisition of ECG signals

2. BIO-MEDICAL INA ARCHITECTURES

The conventional instrumentation amplifier (IA) configuration, as depicted in Figure 6, has limitations when applied in the biomedical field. Directly connecting resistors and amplifier nodes introduces significant thermal noise. Additionally, the IA's floating negative inputs necessitate a reference voltage or common-mode negative feedback for biasing. Achieving a high Common-Mode Rejection Ratio (CMRR) [6]. relies on well-matched internal resistors. However, this IA topology is not particularly power-efficient, as energy must pass through resistors to maintain voltage feedback.

Because power must pass via resistors in order to maintain the voltage feedback, this IA is not very power efficient. Given that electricity is necessary for In order to overcome the aforementioned problems, this IA is not very power efficient because energy needs to flow via resistors in order to maintain the voltage feedback. These architectures may be divided into three classes.

1. INA with a DC coupling
2. INA with digital support
3 .INA with an AC coupling

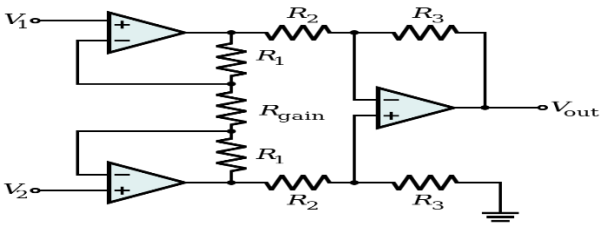

Figure 6: Traditional INA circuit

2.1 INA with a DC Coupling

There is a minimum electrode offset tolerance in the DC-coupling INA design. However, as seen in Figure 7, an LPF is typically employed in the feedback to construct a DC-servo loop that filters DC offset.

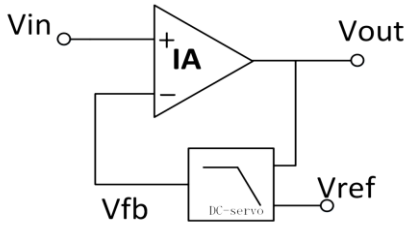

Figure 7: INA circuit for DC-Coupled DC servo loop.

2.2 INA with a AC Coupling

The AC-coupling IA architecture, as shown in Figure 8, is also frequently utilized in Bio signal acquisition integrated circuits. This INA's high-pass curve low-frequency is made to use a feedback loop to filter out significant DC electrode offsets. The input resistor needs to be quite large to achieve the transmission function and lower thermal noise.

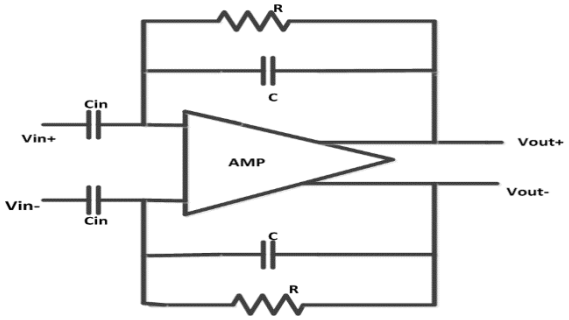

Figure 8: INA circuit with AC coupling

2.3 INA with Digital Support

With multiple types of data converters, it is a different system that replaces the DC-servo loop and removes DC offset while keeping the core amplifier. Large input impedance is a feature of this design. With the benefit of area and power efficiency, the DC servo loop [7]. balances negative feedback using an ADC and selects the DC offset through the use of an electronic low-pass filter. The diagram in Figure 9 illustrates the architectural circuit of the digitally assisted INA.

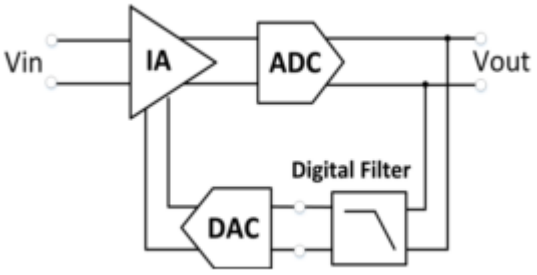

Figure 9: INA circuit with digital assistance

The absence of a unified INA infrastructure has led to various architectural trade-offs. Each architecture has its advantages and limitations. Table 1 summarizes the overall efficiency of the three INA types. When designing, factors like technology, voltage, and power are pivotal in selecting the most appropriate architecture for a particular application.

The INA does not have a best-fit model. Because of the trade-offs between these needs, each INA architecture [8]. has pros and cons of its own. Regarding the INAs' cutting-edge designs mentioned above, a number of architectures have been suggested.

Table 1: Overall effectiveness of three different INA types

Architecture Type / Parameters	DC coupled INA	AC-coupled INA	Digital-assisted INA
Input Impedance	High	Low	High
CMRR	High	High	Low
Noise	Low	Low	High
Power	High	Medium	Low
Electrode Offset Tolerance	-	Medium	Low

3. PROPOSED DESIGN

This section delves into the trade-off between noise and power in instrument amplifiers. While many articles tend to prioritize one over the other, the significance of achieving both low power consumption and low noise in ECG signal collection and monitoring cannot be overstated. Equally crucial is the development of a fully integrated network capable of covering the entire frequency spectrum of a bio-potential ECG signal. This necessitates the utilization of high-value capacitors and resistors to introduce high-pass characteristics with a lengthy time constant. Various methods have been employed to incorporate large capacitors and resistors in order to achieve this desired temporal constant. The objective is to deliver a fully integrated ECG Instrumentation Amplifier (INA) that offers low power consumption and minimal noise, thereby enhancing signal quality and enabling continuous monitoring.

The study aims to enhance overall performance by integrating the AC-coupled technique with chopper stabilization. The primary objective is to combine these two approaches effectively, addressing challenges and achieving essential qualities. Figure 10 illustrates a design configuration featuring an operational transconductance amplifier (OTA) using chopper stabilization and an AC-linked CMFB system. The system's mid-band gain depends on the input-to-output capacitance ratio, and input node capacitances mitigate differential electrode offset effects.

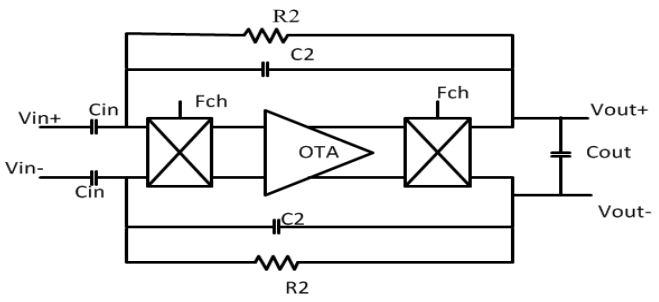

Figure 10: The INA's proposed architecture

The architecture achieves a higher cutoff frequency through a combination of mid-band gain, output capacitance, and OTA transconductance. Conversely, the lower cutoff frequency is determined by the combination of resistors R2 and capacitors C2. By employing an OTA instead of an OP-Amp at the second chopper circuit's output node, the need for an additional filter stage is eliminated. With only one active component—the OTA—the architecture [9]. demonstrates reduced noise, lower power consumption, and a decreased supply voltage. Transistors are designed to be operated in weak or moderate inversion zones to minimize power usage. Researchers have investigated the unified all-regional model (the "EKV Model") to address transistor utilization in the inversion region. The EKV configuration of the MOS transistor is calculated using the following calculations.

$$IC = \frac{I_D}{I_S}$$

$$g_m = \frac{I_D}{\eta \Phi_t} \frac{1 - \exp\left(-\sqrt{IC}\right)}{\sqrt{IC}}$$

$$I_s = 2\mu C_{ox} \frac{W}{L} \emptyset_t^2$$

Where,

Is called as the normalization current.

Drain Current is denoted as $I_{D.}$

I_S is referred as slope factor, its value is between 1 to 1.3.

It is typically interpreted as 1.

C_{ox} is called oxide Capacitance..

$$C_{ox} = \frac{\epsilon_0 \ \epsilon_{si}}{t_{ox}}$$

The permittivity of open space is denoted by ∈_(0), whereas the relative permittivity of silicon is denoted by ∈_(si), with t_oxi denoting the thickness of the oxide layer.

Thermal voltage, or ϕt, is measured at room temperature and is commonly assumed to be 25.6 mv.

The Inversion Coefficient is referred to as IC.

Transistors tend to operate in the strong inversion region when the current gain (IC) is significantly greater than 1. Conversely, they function in the weak inversion zone when IC is much less than 1.

In this short, the drain current ID is assumed to be 2uA. Based on an examination of the voltage-current relationship of an NMOS transistor with W = 1µm and L = 90nm dimensions, the assumption was made. In this work, 45nm CMOS technology is simulated. Since it is assumed that the transistor is operating in the weak inversion area, the drain current that is just below the threshold voltage is taken into account. As a result, a drain current of 2 uA is assumed.

3.1 Transistor Dimensions

Based on the EKV transistor model covered in this chapter, the transistor sizes of the circuit operating in the weak inversion area are provided below. Table 2 displays the various transistor sizes that will be used in the suggested instrumentation amplifier. The transistor's channel length may be selected by the designer in accordance with pertinent design elements. Multiplying the technology used ten or thirteen times during the design process yields the maximum length of a transistor.

Table 2: Different Transistors' Transistor Dimensions

Device	Dimensions(W/L)	Tail current(I_D)
Mtail(OTA)	19.2/1	2µA
M1	9.6/1	1µA
M2	4.06/1	1µA
M3	4.06/1	1µA
M4	9.6/1	1µA
M5	4.06/1	2µA
M6	4.06/1	-
Mtail(CMFB)	9.6/1	2µA
M7	4.06/1	-

4. SIMULATION RESULTS

Tanner EDA tools are used in this work to simulate in CMOS 45nm PTM technology files.

4.1 The OTA

As illustrated in Figure 11, the AC research indicates that the OTA has a DC gain of 47dB. Of the various blocks that make up the suggested INA design, the OTA uses the most power.

The power consumption of the INA is primarily determined by the OTA. When transistors operate in the weak inversion zone or are active, power usage decreases significantly. Additionally, efforts are underway to reduce noise originating from the OTA, which is the primary noise source in the INA.

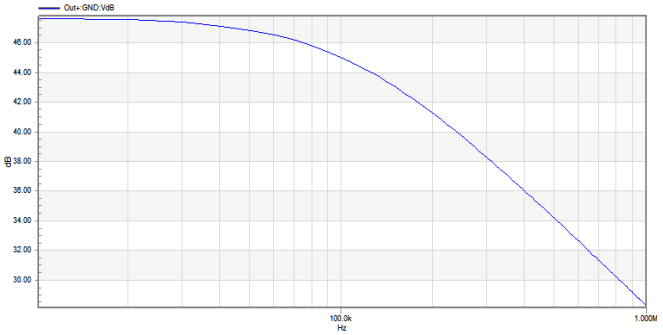

Figure 11: Response of the Proposed OTA to Frequency

4.2 The Final Results Of Ina

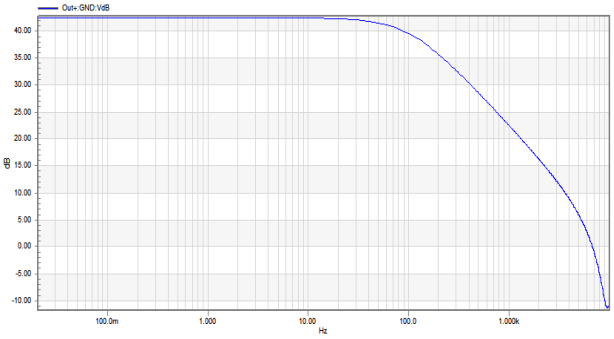

Figure 12: The Proposed Instrumentation Amplifier's (INA) Frequency Response

A bandwidth of 0.005–100 Hz is expected for the suggested instrumentation amplifier in order to obtain and monitor ECG signals accurately. The cout is selected based on the planned higher and lower cutoff frequencies, R2 and C2 values. In the INA simulation, C2=1mF, R2=31.8K, and Cin=2PF are the resistors and capacitances that are used. The impact can be mitigated by reducing the input capacitance. A 2PF capacitor is therefore selected.

Figure 12 displays the fully integrated INA's frequency response. For any ECG application, this shows that INA achieves an amazing 44dB gain with a bandwidth spanning from 0.005Hz to 100Hz.

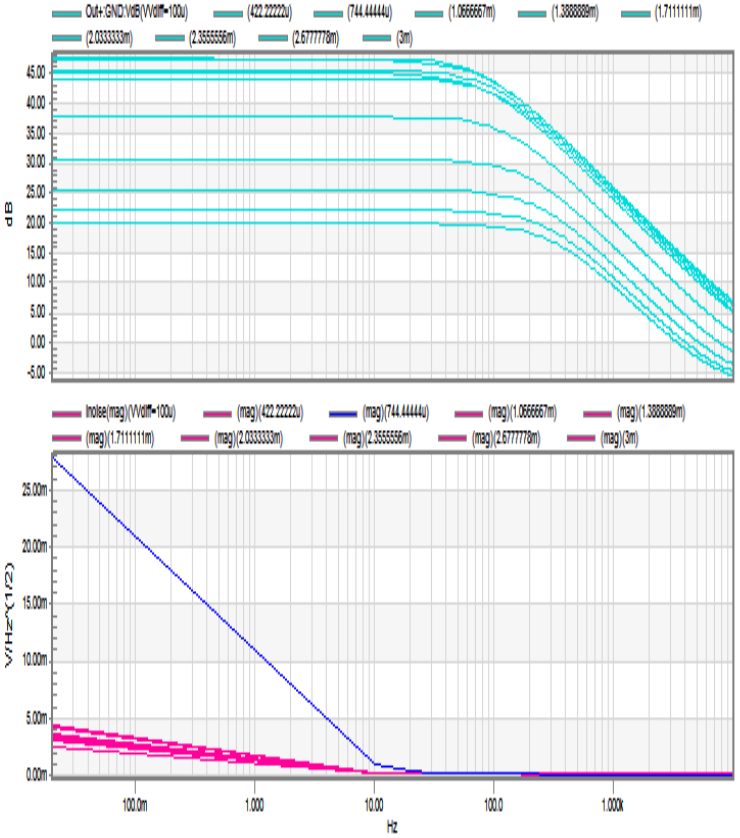

Figure 13: Variation between the Instrumentational Amplifier's gain and input noise in relation to its differential voltage.

Figure 13 illustrates that as the differential input voltage increases, the gain decreases. Simultaneously, there is an increase in input-referred noise. To achieve the desired noise voltage spectrum density and gain for the output, the differential input voltage of the Instrumentation Amplifier is adjusted from 100 µV to 3 mV. The observed input noise voltage spectrum density is 92 nV/√Hz. On average, the increase in noise was approximately 38 dB. The bandwidth at 38 dB on the plot is approximately 130.

The RMS value of this spectral density is $V_{onoise,}$

$$_{RMS}=\sqrt{\int_{fl}^{fh} V_{inoise}^2} \qquad ...4.25$$

=

$$V_{inoise}\sqrt{BW}_{=} = 1.1\mu rms \quad ..4.26$$

Figure 14 illustrates the transient analysis of the recommended INA. The INA is subjected to a 2 mVpp sinusoidal input signal at a frequency of 10 Hz. Notably, when the signal is amplified to an output voltage of 200 mVpp, minimal noise is observed.

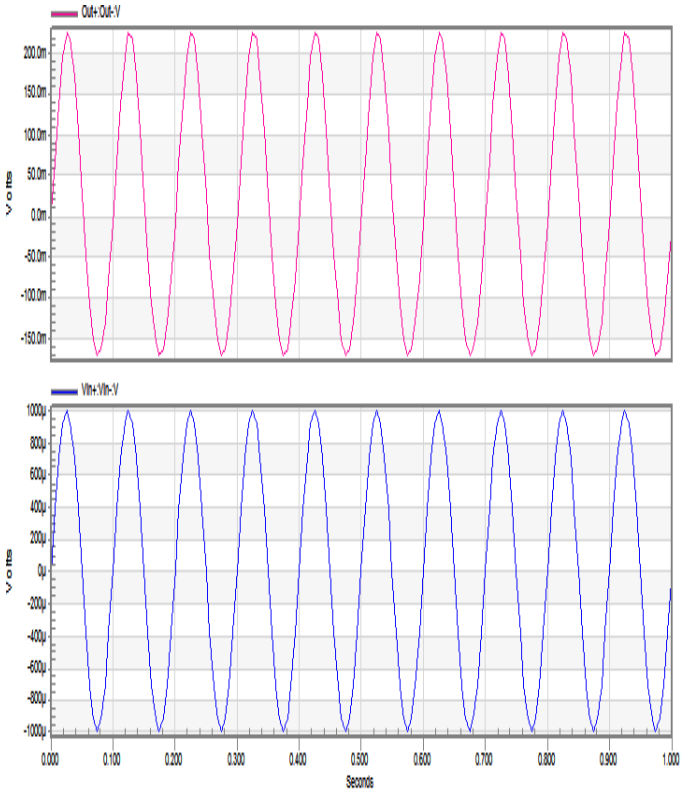

Figure 14: Analysis of Transients in the Proposed INA

Table 3: An overview of the performance criteria in the suggested INA

Parameters	**Result**
Gain	45db
Bandwidth	0.005-100Hz
Input Referred Noise	1.1µVrms
Power Consumption	0.271µW
CMRR	>75dB

The INA delivers more than 75dB of CMRR within the selected bandwidth. For the application, the acquired parameters are excellent. The design's current feedback system produces a high CMRR rating. Since the total power usage is only 0.271uW, the recommended INA is a better option for acquiring, monitoring, and amplifying the ECG signal.

Table 3 summarizes the measured performance characteristics of the recommended Instrumentation Amplifier (INA). Meanwhile, Table 4 provides a comparison between the proposed study's results and those of advanced instrumentation amplifiers commonly used in biological applications. The suggested low-noise, low-power CMFB instrumentation amplifier is specifically designed for ECG signal monitoring. Notably, the INA achieves a high Common-Mode Rejection Ratio (CMRR) exceeding 75 dB. The CMRR is influenced by both common-mode and differential signal amplitudes.

Table 4: The proposed INA design is contrasted with current architectures

	[Ref 56]	**[Ref 57]**	**[Ref 58]**	**[Ref 46]**	**[Ref 47]**	**This Work**
Name of the IA	Two Stage Chopper Current feedback IA	Inverting AC-Coupled Chopper IA	Chopper Stabilizer IA	Feedback Configuration band pass IA	Capacitive Coupled chopper IA	Chopper based CMFB IA
CMOS Technology(µm)	0.7	0.18	0.13	0.13	0.13	0.045
Supply Voltage(V)	5	1.8	1	2	1.2	0.8
Noise(µVrms)	2	1.75	2.18	3.2	1.3	1.1
Band Width(Hz)	0.5-100	0.5-100	0.5-100	0.9-350	0.5-100	0.5-100
CMRR(db)	137	84	125	95	98	>75*

Within the ECG frequency range of 0.5 to 100 Hz, the input-referred noise measures approximately 1.1 µVrms. In comparison to several advanced instrumentation amplifier designs, the suggested architecture demonstrates superior Common-Mode Rejection Ratio (CMRR) and minimal noise levels.

5. CONCLUSION

The scalability of the new analog front end for ECG signal collection faces challenges related to low noise and low power consumption. This study proposes an instrumentation amplifier (INA) designed to gather, amplify, and track ECG data. By employing the AC-coupled Chopper stabilization technique, the INA achieves both low power consumption and minimal noise. The architecture provides the necessary high-pass response for ECG applications, with a bandwidth spanning 0.05 Hz to 100 Hz, a 45 dB gain, and a power consumption of 0.271 µW. However, the INA's effectiveness is constrained by the development of parasitic resistance induced by chopping.

Designing comparators using submicron CMOS technology presents challenges due to restricted common-mode input and low power at lower supply voltages. The threshold voltage of transistors may not scale down effectively. To address the reduced rail-to-rail voltage, larger transistors are employed, potentially increasing die size and power consumption. Existing literature on low-voltage and low-power CMOS comparator design suggests two approaches: novel technical solutions and circuit-level modifications to achieve scalability.

Technological advancements have not only resulted in creative circuit designs to address a variety of deep sub-micron technology concerns (problems and challenges), but they have also managed to manage lower voltage without complicating easily accessible or existing circuits. In order to regulate and optimize a variety of performance metrics, such as area, PDP, strength, offset, speed, and kickback noise, several design changes are suggested in the literature.

5.1 Future Scope

One circuit may be developed in the future to detect all bio-signals. Moreover, an FPGA board's on-chip peripherals may be used to build an ECG signal detection circuitry. In

addition, as technology advances more quickly, creative new solutions and design components might be developed to meet scalability requirements. Researchers may also focus on CMOS IC design techniques with a high level of assurance and power efficiency for the wireless healthcare and medical application sectors as CMOS technology advances. Building methodologies can be developed at both the circuit block and system levels over the entire technological breakthrough foundation. methods for creating ultra-low-power CMOS circuits that are placed strategically at low-technological nodes to maximize the network impact of wireless health and medical services.

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