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A Wideband 4-Level Frequency-Shift Keying Demodulator for Biomedical Implants

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ABSTRACT

A wideband 4-level frequency-shift keying (FSK) modulation scheme for biomedical implants is investigated and its digital demodulator circuits have been implemented with a 0.18μm 1P6M standard CMOS technology process. The application of the implementation technique is transferring data to wireless biomedical implants at a higher data-rate modulation scheme of 4-level FSK. The proposed demodulator circuits have been validated with test chip measurement results. It consumes the power of 7.2mW from a 1.8V supply.

Key words: 4-level FSK, biomedical implants, digital demodulators, CMOS.

1. INTRODUCTION

A high data-rate transmission is highly desired for the wireless biomedical implants, especially for those that interface with central nervous systems such as cochlears [1]-[5] which requires a large amount of data to simultaneously interface with even more amount of neurons through many channels. For wireless communication standards such as IEEE 802.11a however, the data rate can be as high as 54 Mbps with the expense of high carrier frequency even up to 5.8GHz. However, a high data-rate-to-carrier- frequency ratio with FSK modulation even up to 67% can be found in [6]-[7] at the expense of high frequency deviation (or poor spectrum efficiency) up to 2.5MHz (2-level FSK modulation scheme with 2 carrier frequencies, f_1=5MHz for logic "1" and f_0=10MHz for logic "0"). In this paper, the 4-level frequency-shift keying (FSK) modulation scheme is utilized, which the better performance in terms of circuit simplicity and higher data-rate can be validated with the proposed circuit experimental results.

2. THE PROPOSED 4-LEVEL FSK DEMODULATOR

The input RF signal is firstly down-converted to IF signal by using a down-conversion mixer and amplified to full-swing signal with an IF OTA. The demodulation is finally performed with a digital demodulator and converted back to digital data. Figure 1 illustrates the block diagram of the proposed 4-level FSK demodulator.

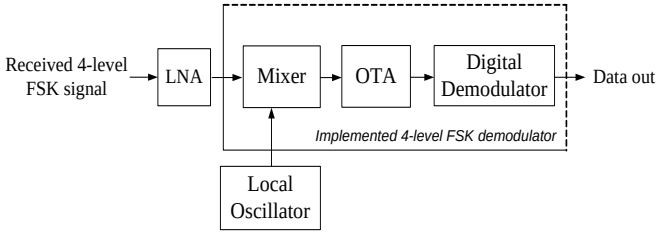


Figure 1: Block Diagram of the Proposed 4-Level FSK Demodulator

2.1 Mixer

The received RF signal is down-converted to IF signal with the double-balanced mixer as shown in Figure 2, in which a fully-differential configuration is employed [8]-[9]. It mixes the differential input RF and LO signals and develops the differential output IF signal. In Figure 2, the resonator pairs (L1, C1) and (L2, C2) act as the differential output loads in order to obtain a higher conversion gain. VBP is the bias voltage with bias resistors Rp1 and Rp2. R5 and R6 are the bias resistors providing the maximum DC level for the LO oscillator. The voltage dividers constructed with resistors R1, R2 and R3, R4 bias the differential RF port at 1V. The degenerative resistor RDeg is connected across the path between the current-mirror stages (M1 and M2) and the trans-conductance stages (M3 and M4). Thus, it does not lead to the voltage drop and still has the same linearity enhancement.

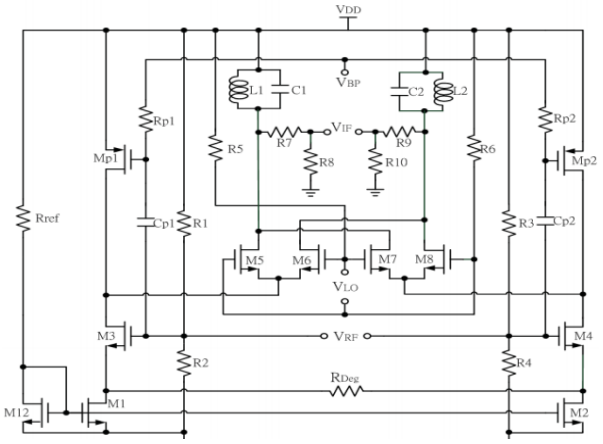


Figure 2: Circuit of the Double-Balanced Down-Conversion Mixer.

2.2 Operational Transconduction Amplifier (OTA)

In order to perform digital demodulation, the down- converted IF signal has to be full-swing with the further amplification. An OTA is employed to amplify the IF signal. Figure 3 shows the circuit of the OTA. Table 1 illustrates the performance of the OTA.

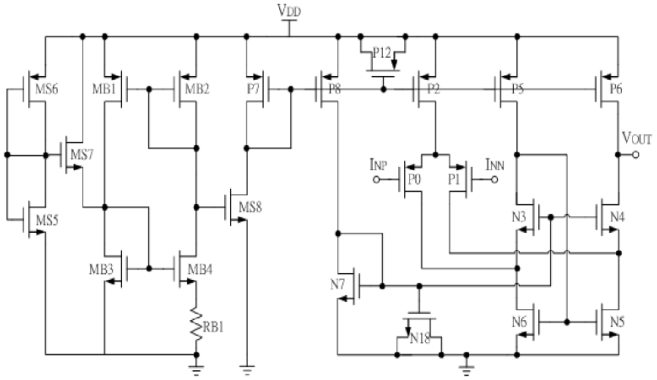


Figure 3: Circuit of the OTA

Table 1: Performance Summary of the OTA

DC Gain	51.1dB
-3dB Frequency	4.24MHz
Unity Gain Bandwidth	455MHz
High Frequency Gain	-16.2dB

2.3 Digital Demodulator

In the proposed digital approach for FSK demodulation, the periods of the four down-converted intermediate- frequency (IF) carriers are measured by the employment of a binary counter triggered with higher frequency clock, which is similar to the previous publication [6] whereas in our approach we measure the whole period which can have more duration to discriminate between the four IF carrier frequencies. In theory, the relationship between the clock frequency and the four IF carrier frequencies can be described as follows,

$$\frac{1}{f_{clk}} < \left(\frac{1}{f_{IF(k+1)}} - \frac{1}{f_{IF(k)}} \right), \quad k=1, 2, 3 \qquad (1)$$

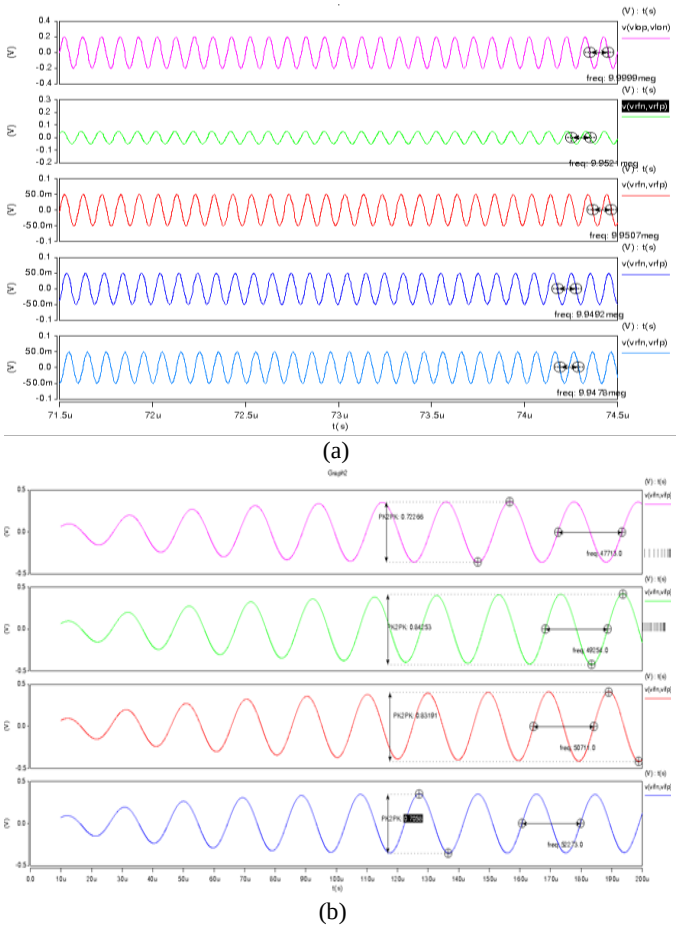
Moreover, the minimum width of the counter n is required to satisfy the relationship indicated in the follows,

$$\frac{f_{clk}}{f_{IF4}} < 2^n \qquad (2)$$

Based on (1) and (2), we employ a 7-bit counter operating at 5MHz to measure the period of the received down-converted FSK full-swing signal. Note that by the employment of a 7-bit counter with 5MHz clock, it can count the longest period from the down-converted IF signal with 47.6 KHz. Also, the four different periods can represent the two-bit received data.

3. EXPERIMENTAL RESULTS

The circuit simulation of the mixer has been performed with Hspice. The amplitude level of the four RF input signals is 50mV with frequencies 9.9524 MHz, 9.9508 MHz, 9.9492 MHz, and 9.9476 MHz. They are down-converted with a local oscillator which has 200mV amplitude, 10 MHz frequency as indicated in Figure 4(a). Also note that the supply voltage V_{DD} is 1.8V and a bias voltage V_{BP} is 0.806V. The down-converted IF signals can be obtained with the frequencies 47.6 KHz, 49.2 KHz, 50.8 KHz, and 52.4 KHz, which the amplitude is near 386mV as shown in Figure 4(b).



(a)

(b)

Figure 4: Simulation Waveforms (a) the Input RF Signals (b) the Down-Converted IF Signals

Figure 5 shows the simulated waveforms of the digital demodulator. Four carrier frequencies of the received down-converted FSK signals, 52.4 KHz, 50.8 KHz, 49.2 KHz and 47.6 KHz represent received demodulated data 2'b11, 2'b10, 2'b01, and 2'b00, respectively and the counter will detect and measure the periods of the FSK carrier signals.

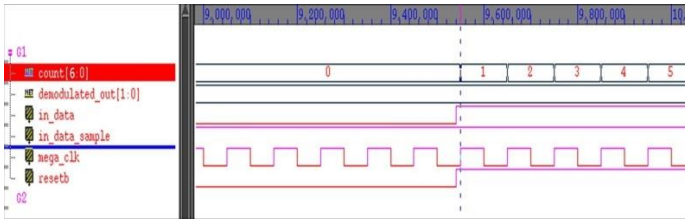


Figure 5: Simulation Waveforms of the Digital Demodulator

Figure 6 shows the microphotograph of the implemented demodulator with the TSMC CMOS 0.18μm 1P6M technology process, T18 provided through the CIC foundry service, in which the die size is 563.44 × 628.59μm^2.

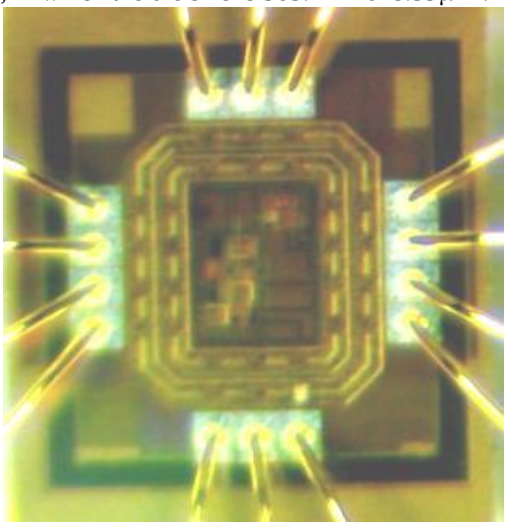
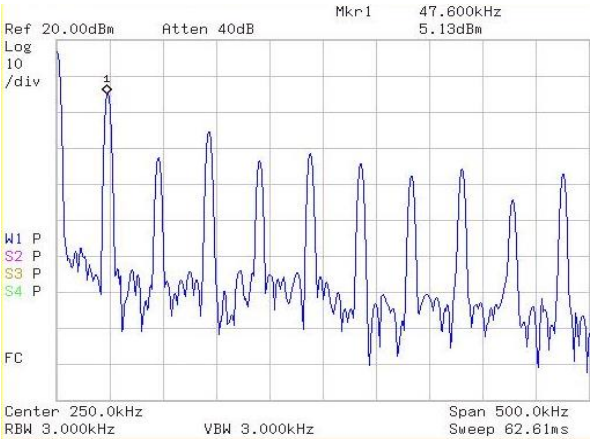
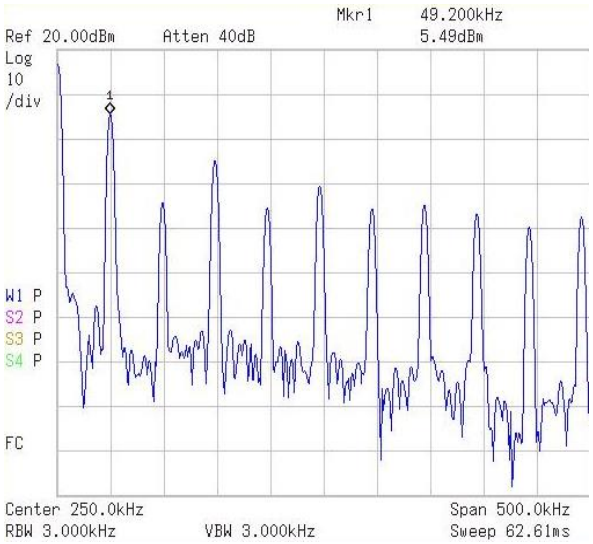


Figure 6: Die Microphotograph of the 4-Level Frequency-Shift Keying Demodulator

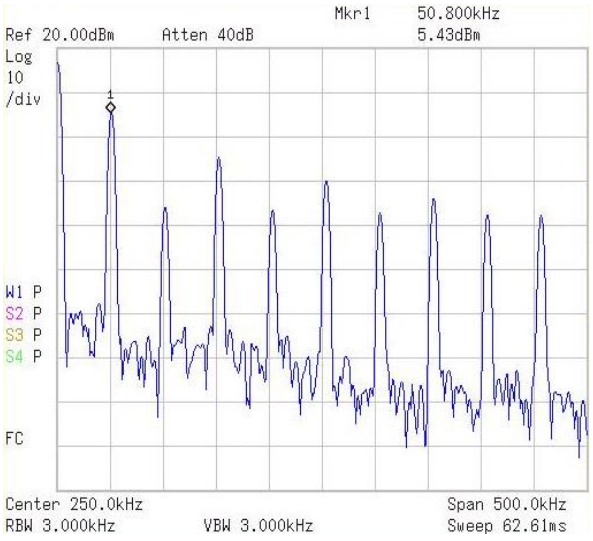
The measurement results of the down-conversion mixer are shown in Figure 7. Obviously, the down-converted IF signals are much higher than their harmonics for each case.



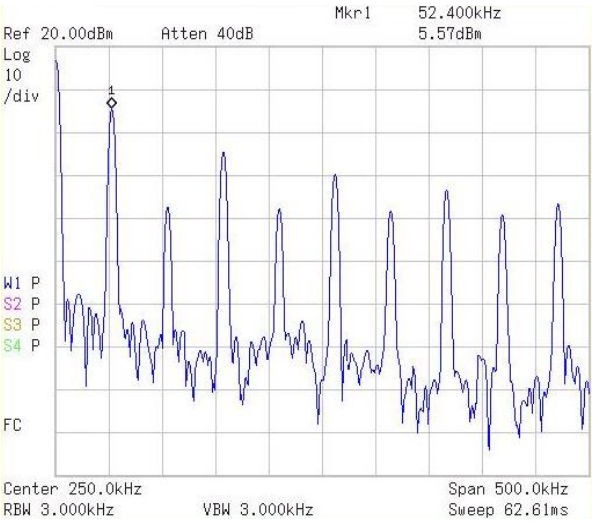
(a)



(b)



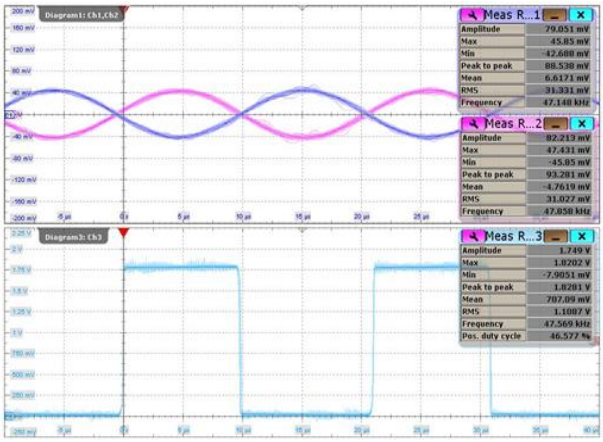
(c)



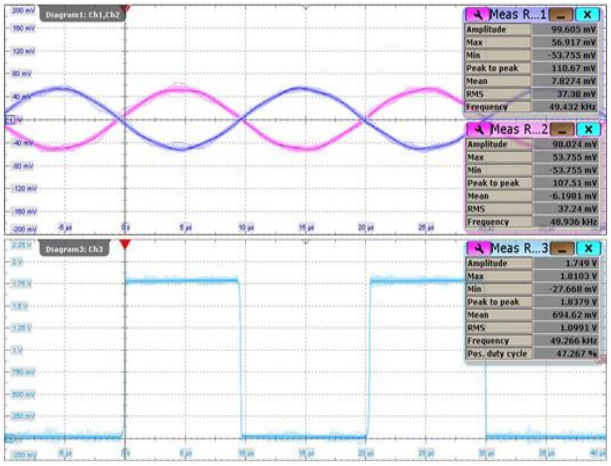
(d)

Figure 7: Measurement Results of the Down-Converted IF Spectra for RF Input Signals with the Frequencies, (a) 9.9524MHz (b) 9.9508MHz (c) 9.9492MHz (d) 9.9476MHz.

The measurement results of the OTA output clock signals are shown in Figure 8. The upper channel shows the differential input of the OTA and the lower channel indicates the single-ended output full-swing signal of the OTA for the next digital demodulator stage.



(a)



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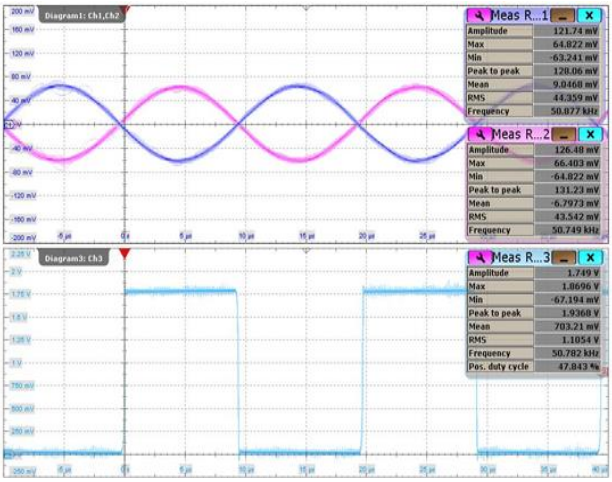

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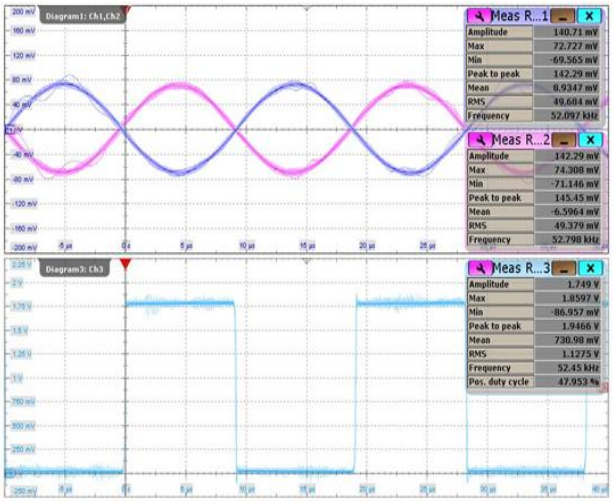

(d)

Figure 8: Measurement Results of the OTA Time-Domain Output Clock Signals (Lower Channel) with the Output Frequencies, (a) 47.6KHz (b) 49.2KHz (c) 50.8KHz (d) 52.4KHz.

The implementation of the digital FSK demodulator has been performed with Verilog HDL and synthesized with Synopsys Design Compiler. In order to provide bit error tolerance due to the received IF signal jitter, the circuit design can tolerate two-bit error. In other words, we can obtain count '105' for a 47.6 KHz IF signal with the input 5MHz-clock signal for the counter. However, due to the jitter effect on the received 47.6 KHz IF signal, the count can be ranged between '104' and '106', which is equivalently near ±0.53KHz frequency deviation. Under this circumstance, the same code will be assigned. Moreover, larger jitter tolerance can also be achieved by the employment of higher-frequency clock for the counter whereas it can consume more power. Table 2 reveals the specifications of the 4-level FSK demodulator circuits and Table 3 summaries the performance of the realized chip.

Table 2: The Specifications of the 4-Level FSK Demodulator Circuits

Character	Frequency
Received RF Signal Frequency	f_{RF1}=9.9476 MHz f_{RF2}=9.9492 MHz f_{RF3}=9.9508 MHz f_{RF4}=9.9524 MHz
Down-Converted IF Signal Frequency	f_{IF1}=52.4 KHz f_{IF2}=50.8 KHz f_{IF3}=49.2 KHz f_{IF4}=47.6 KHz
Local Oscillator Frequency	10MHz
Frequency of V_{IF} versus Binary Code	f_{IF1}=52.4KHz = 1011111 f_{IF2}=50.8 KHz = 1100010 f_{IF3}=49.2 KHz = 1100101 f_{IF4}=47.6 KHz = 1101001 Other Frequencies = 0000000

Table 3: Performance Summary

Technology	TSMC CMOS 0.18μm, 1-poly, 6-metal
Modulation Scheme	4-level Frequency-Shift Keying
Modulation Index	0.02
Supply Voltage	1.8V
Operating Frequency	10MHz
Power Consumption	7.2mW
Die Size	$0.563\times0.628mm^2$

4. CONCLUSION

We have proposed a 4-level FSK digital demodulator for wireless operation of biomedical devices and furthermore, the preliminary feasibility has been validated with the experimental chip measurement results. Future work of this research is then going through with the implementation of even more integrated functional blocks on the test-chip and its measurement results may further confirm the correctness of the proposed architecture.

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