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Analysis and Reduction of high power consumption using parallel prefix adder

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ABSTRACT
An unconventional non-weighted number system that has gained a great scientific interest is the RNS (residue number system) that is high speed arithmetic, proficient of parallel, and carry-free. It utilizes number residues, in specific modulus for its representation. The design of reverse converter is based on modular address and regular adders that lead increase in power consumption and low speed. This is the main reason which prevents the use of Residue Number system in many applications. The parallel prefix based adder components is utilized to resolve the consumption issue of high power and supply enhanced trade-off among delay and power consumption.
Keywords: Parallel Prefix adder, Reverse converter, Residue number system

1. INTRODUCTION

In day to day life Embedded systems have been transformed from single-function control frameworks to highly complex system. Embedded systems like the portable multimedia and communication gadgets, personal wireless communication have created stringent requirements such as price, performance, power. These battery-powered gadgets have created a demand for low-priced, power efficient and high performance embedded processors [1-3] The RNS (residue number system) plays a major role in such devices due to competitive delay and low power feature. The RNS was used in the execution of fast arithmetic and fault tolerance in digital systems. The RNS requires forward and reverse conversion. However in reverse conversion the conversion stages are very critical in the evaluation of presentation of overall RNS. [4] Compared to other step reverse conversion leads to more delay. Hence the reverse conversion process initiates more overhead in terms of complexity and speedis more difficult in computation of the process. To develop the presentation of the converters, well-known adder architectures were used. To execute CPAs (carry-propagate adders), such as ripple-carry architectures and CSAs (carry-save adders) is used. The ones with parallel-prefix architectures are the fastest and expensive adders. The parallel-prefix adder [5] usage is to execute converters highly rises the speed and reduces the consumption issue of the power.

2. RELATED WORK

The residue number system encodes a huge number into a small numbers which consequences in substantial speed up of complete data processing. Each large integer might be portrayed as a set of smaller [3] integers named the residues. Three main steps involved in RNS are forward conversion, arithmetic computation and reverse conversion. The process of encoding input data into RNS representation is known as forward conversion. This procedure can be done by dividing the given conventional number by the entire module in the module set and finding the remainders of the divisions. The Reverse [5] Conversion is the procedure of converting RNS representation into conventional representation. Distinct module sets have to be chosen as shown in figure 1. The hardware modules assortment is a key to the performance of RNS. The use of parallel prefix adder based on different architecture with distinct structure such as Kogge–Stone (KS) and Brent—Kung adder shows a significant increase in performance [6].

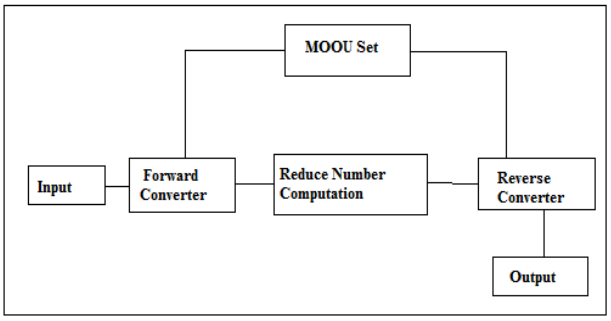

Figure 1: Block Diagram of RNS system

2.1 Parallel Prefix Adder

The quicker operation in reverse converter design was achieved with the help of parallel prefix structure.

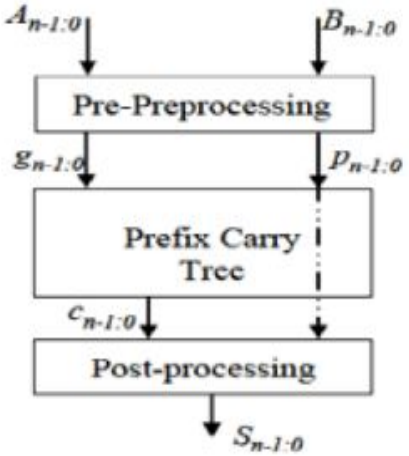

Figure 2: Block diagram of parallel prefix structure

As in figure 2 there are three main blocks in parallel prefix structure; they are prefix carry tree, pre-processing block, and post processing block. The procedure of the adder initiates with pre-processing phase [7] [11] by producing the Propagate (Pi) and Generate (Gi) shown in (eq 1), (eq 3). In prefix carry tree the prior block signal output all carry the bit signal. These stages comprise 3 logic complex cells. They are Buffer cell, Grey cell, and Black cell. The Grey cell performs only generate (G(i,j)). The black cell is used to calculate the propagate (P(i,j)), and the generate (G(i,j)) are shown in the (eq 3), (eq 4). The post processing block obtains the carry bits produced in the 2^{nd} phase, which produces the sum and the equation is given [8]. The block diagram is shown in the Fig1

$$G_{m:n}=A_n \cdot B_n \quad \ldots.(1)$$
$$G_0=C_{in} \quad \ldots.(2)$$
$$P_{m:n}=A_n \oplus B_n \quad \ldots.(3)$$
$$P_0=0 \quad \ldots.(4)$$
$$G_{m:n}=G_{n:k} + (P_{n:k} \cdot G_{k-1:n}) \quad \ldots.(5)$$
$$P_{m:n}=P_{n:k} \cdot P_{k-1:j} \quad \ldots..(6)$$
$$S_n=P_n \oplus C_{in} \quad \ldots.(7)$$

We might reduce power consumption and attain the high speed in the system with the use of Brent Kung adder prefix structure. BK adder is selected mostly for smallest fan-out and high speed in operation compared to other parallel prefix adder structure [9]. For instance, as in Figure 3 depicts the BK adder prefix structure with 3 main cells in the prefix structure.

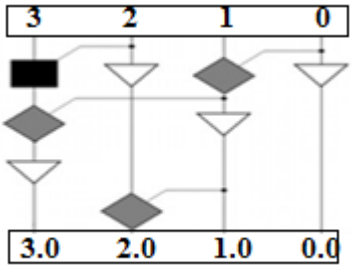

Figure 3: 4-bit BK adder prefix structure

3. DESIGN METHODOLOGY

4.

The procedure of designing a reverse converter is defined in this section. The selection of moduli set is the initial step involved in a reverse converter design. The moduli set selection is used to determine RNS's hardware realization, dynamic range, and the speed. The 3 moduli set (2^n-1, 2^n, 2^n+1) were considered for the design, where n is a natural number. The importance of these moduli set is that they might be proficiently executed utilizing binary hardware, which leads to simple design and provides advantages of speed cost. The moduli values of the moduli set and the residue numbers must be substituted in CRT conversion procedure formulas. Here the residue number is the yield of the forward converter. The CRT conversion algorithm involves the calculation of recursive moduli inverse. The best way to implement moduli inverse is to save the constant in ROM, [10] which is then multiplied with the residue number and then added using the adders. Arithmetic properties and propositions are used for simplifying the resulting equations. The final equations are realized by adder components like CPA-EAC, CSA-EAC, PPA, and CPA. The above said procedure is consolidated as the following algorithm.

Step 1: Set the input

Step 2: Set the moduli set.

5. RESULTS

The circuit might be quantified and designed in Verilog. The modulus set (2n-1, 2n, 2^n+1) was chosen. The Proposed system is simulated and verified using Model Sim ALTERA STARTER EDITION 6.4a. The below simulation result shows the output of the system as in figure 4 with n=2 for the above module set.

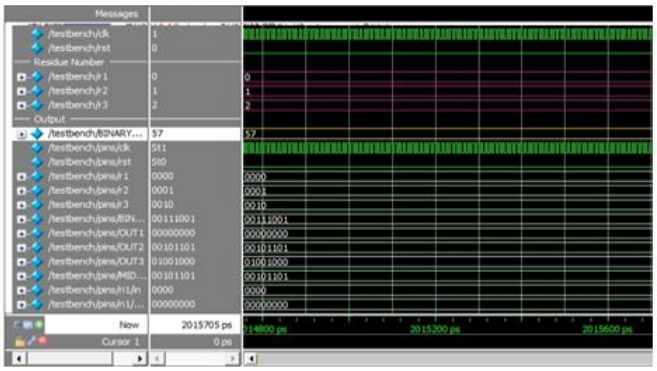

Figure 4: Simulation Output

The following Table represents the comparison of adders in terms of delay and frequency which is calculated using the tool Xlinix ISE 14.2 for the target device xc3s400e-5tq144.

Table 1: Comparison of Adders in terms of Delay and Frequency

ADDER	DELAY(ns)	FREQUENCY(MHz)
RCA	12.804	78.102
CLA	7.765	128.785
CSA	7.626	131.129
KS	2.257	443.095
BK	2.021	494.841

Shown the above table 1 it has compare adders in terms of delay and frequency

6. CONCLUSION

In this paper the reverse converter was simulated. The above result shows that the reverse converter simulated using the BK parallel prefix adder network has less delay compared to other adders. The reverse converter was simulated for the {2^n-1, 2n, 2n+1} module set. This shows that the delay is reduced and the efficiency was improved.

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