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Relative and Analytical Review of Quantum Dot Cellular Automata Method Based on 2:4 Decoder Circuits

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ABSTRACT
The Quantum dot cellular Automata technology is used in this manuscript which overcomes the design constraints of nano scale CMOS circuits. This manuscript presents the analysis of 2:4 decoder circuit using four different methodologies. QCA based decoder circuit is implemented using coupled majority voter minority gate, 45^0 rotated cells, multilayer wire crossings and five input Majority Voter gate. Comparative study of these four decoder shows that performance of Coupled majority voter minority gate based 2:4 decoders is good in terms of complexity, latency, and area. The QCA Designer 2.0.3 device is utilized for the implementation of QCA based Decoder circuits.

Keywords: Moore's law, decoder, QCA, Multilayer wire crossing

1 INTRODUCTION

The Moore's law says that, the number of transistors on a unit area doubles every 24 months [1]. The ITRS (International Technology Roadmap for semiconductors) scheme is that the scaling of the CMOS technique will continue till 2019 [2]. Technology that may replace CMOS when the scaling limit is reached is QCA (Quantum Dot Cellular Automata). The QCA technology is built up in cells. Each cell has two electron and 4-5 islands. However due to coulomb repulsion they will always settle down to one of the two stable states that might be labeled as logic „0" and logic „1"as shown in figure1. These are known as binary states. When the cells are placed beside each other, because of Columbic interaction, the adjacent cell will also try to settle to the same logic as that of the first cell. Using these four dot cells binary wire can be obtained, [3] just by placing the cells adjacent to each other.
The advantage of the QCA circuits is that it does not need the power to run the circuit; instead QCA clock will be responsible to trigger the circuit and run it. Figures 1 & 2 represent the 4 stages of QCA clock, they are switch, relax, hold, and release [11], [12].

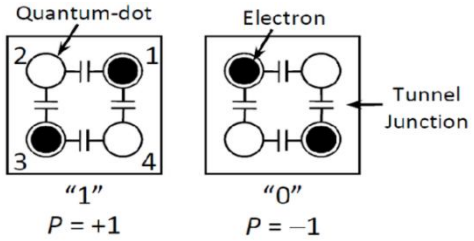

Figure 1: QCA Cell

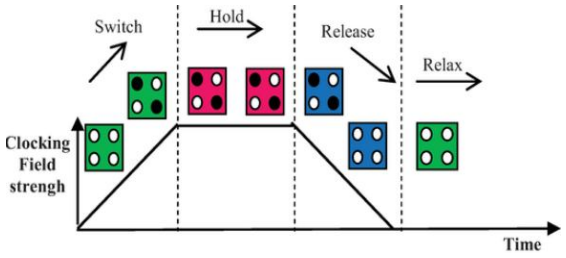

Figure 2: QCA Clock Zones

For the implementation of any QCA circuits basic QCA gates are required. Majority Voter (MV) and Inverter are the basic QCA gates using which any circuit can be implemented. As in Figure 3, Figure 4 depicts the QCA MV gate and Inverters respectively [4].

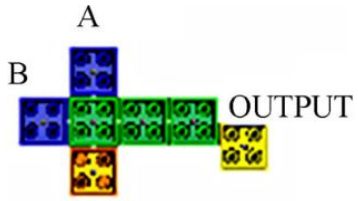

Figure 3: QCA Majority Voter Gate

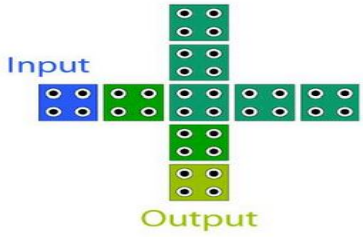

Figure 4: QCA NOT Gate

2 METHODOLOGY

In this paper QCA base 2:4 decoder is implemented with the help of different methodologies.

2.1 Coupled Majority Voter Minority Gate

One of the advantages of CMVMIN gate is that, the number of wire crossings in the circuit can be reduced as well as the number of clock cycles need for the implementation of any QCA based logic circuit will be reduced [13], [14]. CMVMIN has 3 inputs i.e. A,B,C and two outputs F1 and F2. Outputs F1 and F2 are complement of each other as shown in Figure 5.

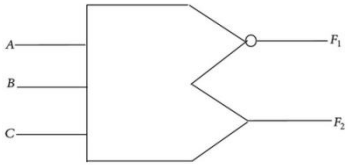

Figure 5: Symbolic representation of CMVMIN Gate and its Equations

Table 1 denotes the Truth table of CMVMIN gate [10]. Here output F1 will be 1 when majority of zeros are there in the input.

Table 1: Truth Table of CMVMIN Gate

A	B	C	F1	F
0	0	0	1	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	0	1

Similarly output F2 wills be1 when majority of the inputs are1.

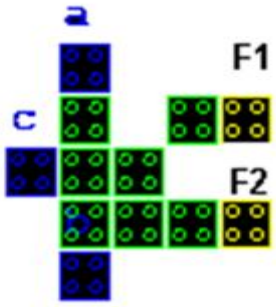

Figure 6: Layout and Simulation Result of CMVLMIN Gate

2.2 45^0 Rotated QCA Wires

QCA wire is made up from the number of QCA cells connected in series. When the cells in QCA cells are oriented by 45^0 and if these 45^0 rotated cells are placed adjacent to each other, it forms a wire. The advantage of this type of wire is that we will get the true and complement value at the output as in figure 6 & 7. If odd number of rotated cells are connected in the wire, it provides the output same as that of input, similarly when even number of rotated cells are connected the wire, it provides the output which is complement of the input [8] [9]. The concept of 45^0 rotated cells is illustrated in Figure 7 and Figure 6.

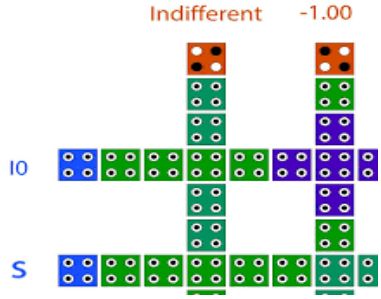

Figure 6: 45^0 QCA wire and wire overlapping

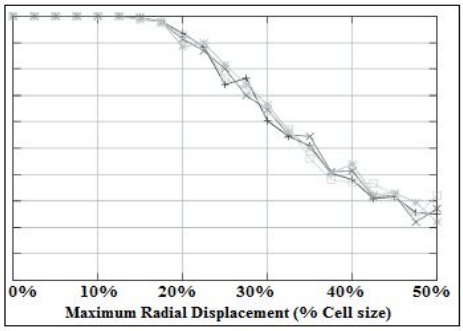

Figure 7: Simulation Result of QCA Wire

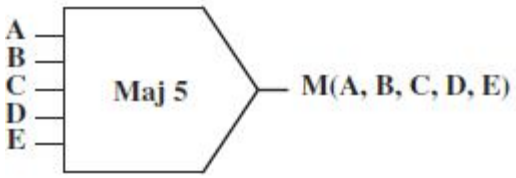

Figure.7: Symbolic representation of 5 input MV gate

Five input MV gate has 5 inputs and one output as shown in Figure 7. Output will be '1' when majority of the inputs are 1. Polarization of input cells is fixed and that of middle cells as well as of output cell can be changed. Layout and simulation result of 5 input MV gate is shown in Figure 10.

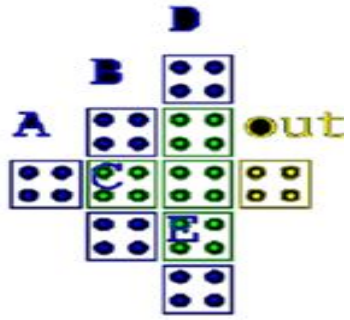

Figure.8: Layout and simulation result of 5 input MV gate

2.3 QCA Based 2:4 Decoder Circuit

As mentioned in section II, four different methodologies are used for the implementation of 2:4 decoder circuits. Here in Figure 9 shows n = 2 and m =4.

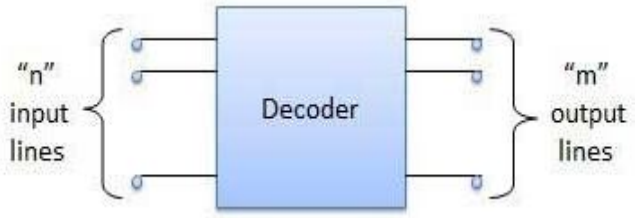

Figure.9: Block Diagram of 2:4 Decoders

3 RESULTS

3.1 QCA based 2:4 Decoder using CMVMIN Gate

QCA based 2:4 decoder circuit is shown in Figuren10. For the implementation of circuit CMVMIN, MV and Not gates are required.

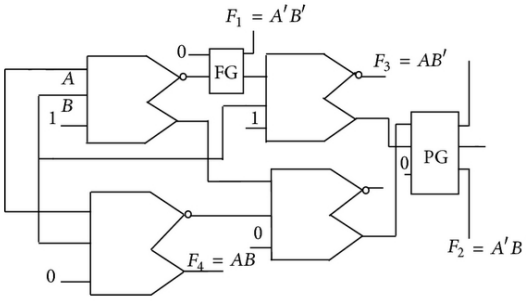

Figure.10: Logical Diagram of QCA based 2:4 Decoder using CMVMIN Gate [5]

Implementation of QCA based 2:4 Decoder using CMVMIN Gate is shown in Figure 11. Only 3 Majority Voter gates, 1 Coupled majority voter minority gate and 2 not gates are required for the implementation of circuit.

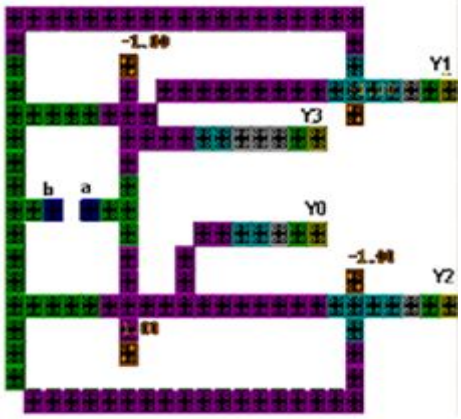

Figure.11: Layout and Simulation of QCA based 2:4 Decoder using CMVMIN Gate

3.2 QCA based 2:4 Decoder using Multilayer Wire Crossings

For the implementation of QCA based 2:4 Decoder using Multilayer Wire Crossings total 8 QCA gates are required i.e. 4 MV gates and 4 NOT gates. Implementation and simulation result is represents in Figure 12.

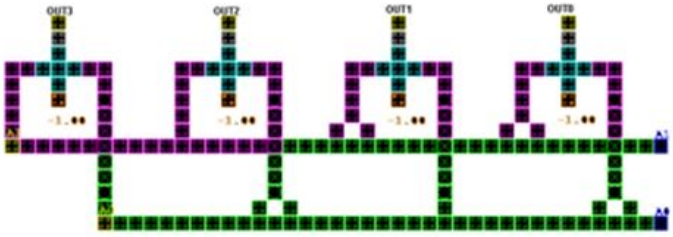

Figure.12: Layout and Simulation result of QCA based 2:4 Decoder using Multilayer Wire Crossings

3.3 QCA based 2:4 Decoder using 5 input Majority Voter Gate

Five input Majority Voter gates and 2 NOT gates are need for the implementation of QCA based 2:4 Decoder utilizing 5 input Majority Voter Gate [9].

4. Analysis

Table 2: Comparison QCA based 2:4 Decoders circuit

QCA Technology	CMVMIN	45^0 rotated	Multilayer	5 Input MV Gate [9]
No. clock	5	4	4	7
Total no of	139	164	208	367
Area	0.33 µm X 0.48	0.76 µm X 0.24	0.86µm X 0.28µm	0.55µm X 0.77µm
Simulation	4 Sec	4 sec	4 sec	5 Sec
Total No. Of devices	Total – 6 1	Total – 8 4 MV 4 NOT	Total – 8 4 MV and 4 INV	Total – 6 4: five input

The above table 2 it has to compare QCA based 2:4 decoder circuits with various inputs.

4. CONCLUSION

Comparative study and parametric analysis of QCA based 2:4 decoder circuit shows that the use of Coupled Majority Voter Minority gate method will provide the fast area efficient circuit as compared to that of other three methods. Complexity of 2:4 decoder circuit using CMVMIN gate is very less as it has only 139 QCA cell count. This circuit is 17% less complex as compared to others. Latency of 2:4 decoder circuit using CMVMIN gate is 5 clock zones, that means it requires one clock zone extra as compared to the decoder circuit using 45^0 rotated cell but it requires two clock zones less when compared to last two methods as shown in Tale 2. Total number of devices required for the implementation of 2:4 decoder using CMVMIN gate is only 5 which is 6 and 8 in other three methods. Hence 2:4 decoder circuit using CMVMIN gate is proved to be efficient in terms of area, speed, complexity and latency, when compared to other three methods. Here it is concluded that CMVMIN gate is used to reduce the number of wire crossings as well as the number of clock cycles need to run the QCA circuit.

REFERENCES

[1] P.K.Bondy,“ Moore‟ slaw governs the silicon revolution,” ProceedingsoftheIEEE,vol.88,no.1,pp.78-81,Aug.2002.

[2] International Technology Roadmap for Semiconductors, Process Integration Devices and Structures (PIDS), http://www.itrs.net/Links/2011ITRS/Home2011.htm, 2011 Edition.

[3] K. Walus, G.A. Jullien, Design tools for an emerging SoC technology: quantum-dot cellular automata. Proc. IEEE 94(6), 1225– 1244(2006 https://doi.org/10.1109/JPROC.2006.875791

[4] M Ozaki, Y. Adachi, Y. Iwahori, and N. Ishii, Application of fuzzy theory to writer recognition of Chinese characters, International Journal of Modelling and Simulation, 18(2), 1998, 112-116. https://doi.org/10.1080/02286203.1998.11760366

[5] Rigui ZHOU, Xiaozhou ,”A Logic Circuit Design of 2-4 Decoder Using Quantum Cellular Automata”, Journal of Computational Information Systems 8: 8 (2012) 3463–3469

[6] K.Walus,“RAM Design Using Quantum-Dot Cellular Automata” ATIPS Laboratory, University of Calgary

[7] Walus K.QCA Designer. QCA Designer website. University of Calgary ATIPS Laboratory. http://www.qcadesigner.ca

[8] M. Malekpour, A Novel Simulation of Decoders using HDLQ in QCA , Canadian Journal on Electrical and Electronics Engineering Vol. 3, No. 7, September 2012.

[9] M. Malekpour and R. Sabbaghi-Nadooshan , “A Novel Simulation of Decoders using HDLQ in QCA”, Canadian Journal on Electrical and Electronics Engineering, Vol.3, No.7, September 2012

[10] Bibhashsen, Sengupta ”Design of Universal Logic Gate Targeting Minimum Wire-Crossings in QCA Logic Circuit”, 2010 IEEE.

[11] KeivanNavi, Razieh Farazkish, et. al. Microelectronics Journal, Elsevier 41 (2010)820–826. https://doi.org/10.1016/j.mejo.2010.07.003

[12] Manisha Waje and Dr. Pravin Dakhole. Design and Implementation of 4-Bit Arithmetic Logic Unit using Quantum Dot Cellular Automata. 3rd IEEE International Advance Computing Conference (IACC) 2013, Pg. 1022 – 1029, doi::10.1109/IAdCC.2013.6514367. https://doi.org/10.1109/IAdCC.2013.6514367

[13] Manisha Waje and Dr. Pravin Dakhole. Design and Simulation of Single Layered Logic Generator Block using Quantum Dot Cellular Automata, IEEE, International Conference on Pervasive Computing -2015, Pg. 1-6, doi: 10.1109/PERVASIVE.2015.7087101.

[14] Manisha Waje and Dr. Pravin Dakhole, Design and Simulation of New XOR Gate and Code converters using Quantum Dot Cellular Automata with reduced number of wire crossings, IEEE, ICCPCT 2014, pg.1245-1250, doi: 10.1109/ICCPCT.2014.7054942.

[15] Bhavana Godavarthi[1],, Papa Rao Nalajala, M Lakshmi Ravi Teja,”Wireless Sensors Based Data Acquisition System Using Smart Mobile Application”, International Journal of Advanced Trends in Computer Science and Engineering, Vol.5 , No.1, Pages : 25-29, 2016

[16] S Deepthi, G Mary Swarnalatha, Paparao Nalajala,”Wireless Local Area Network Security Using Wpa2-Psk”, International Journal of Advanced Trends in Computer Science and Engineering ,Vol.5 , No.1, Pages : 41-45, 2016