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Signal Processing Electrocardiogram using Wavelet Transform Based on Mallet Fast Algorithm

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ABSTRACT
There has been requirement to evolve a general parallel architecture for concurrently processing Electrocardiogram (ECG) using Wavelet Transform based DSP algorithms. In order to acquire spatial ECG electrical signals, 12 ECG lead channels need to be digitized and concurrently processed by Wavelet Transforms, simultaneously acquiring from all the 12 leads. More over now a day 15 Channel ECG is also under consideration in research, for on-line monitoring of critical patient in an ICU situation, while assessing or monitoring load on heart, during treatment process. In this wavelet transform algorithms, matrix inverse operations using wavelet bases matrix, requiring simultaneous matrix multiplications are involved. In order not to loose, high frequency components of ECG, for signal perception or deviation detection using wavelets, the ECG beat is segmented into 410 cubic splines at 2048bps sample rate, to explore association of ECG deviations to different heart ailments. Each spline has associated wavelet coefficient matrix, computed using bases matrix and incoming Digitized ECG vector matrix. On each of the12 lead ECG channels, there are 410 matrix operations required per channel per beat. These matrix operations are required simultaneously, on all the 12 lead ECG Channels, for concurrent digital signal processing of channels for deviation detection. In this processing, multiple data has to be processed by single instruction or algorithm statement, which leads to SIMD (Signal Instruction Multiple Data) architecture. So, a parallel architecture with 16 Processing Elements (PE) with array multipliers for matrix operations are evolved in this review article for suggesting a general parallel architecture for ECG Wavelet Analysis for Signal Perception and Deviation Detection. Using this general parallel architecture, several Wavelet Transform based algorithms, for signal perception for deviation detection are possible, for associating ECG deviations to different heart ailments and localize the deviation to mechanical functional deviation of the hearts anatomy or muscle for on-line diagnostic purpose. So a complete architecture is evolved for such parallel processing, searching the architectural research space and suggested architecture, illustrating brief part of an algorithm.

Keywords: ECG, Wavelet Transform, Cubic Splines, Processing Element, SIMD, Parallel Processing

1. INTRODUCTION

The ECG signal analysis is widely used for the cardiac disease diagnostics and consequently for urgent treatments of ill or critical patients. There has been requirement to evolve good parallel architectures to embed wavelet transform algorithms for analyzing medical signals, specifically ECG, considering, on-line monitoring requirement as an aid in the treatment of patient in an ICU situation. Electrocardiogram (ECG) is generally obtained by 12 lead ECG channels using body area electronics. A 15 lead ECG is also under research, for improved diagnostics, during monitoring of a patient under treatment, for heart preload variations.

The standard ECG wave is a representation of heart's electrical activity, recorded from electrodes on the body surface [1]. The mechanical motion of the heart or polarization and depolarization of the heart muscles that makes it pump blood is represented by ECG Waveform, measured on the body. Deviation detection of ECG Waveform using Wavelet Transforms has diagnostic value, in knowing the difference in heart muscle based pumping action or function. On-line analysis, using Wavelet Transforms provides aid in treating critically ill patients. Many algorithms are in the research space, to apply on ECG waveforms. But, complete ECG is represented by 12 lead or future 15 lead waveforms, which need to be concurrently subjected to Wavelet Transforms based DSP algorithms, simultaneously acquiring and digitizing all the channels. When segmented into spline based wavelet coefficient matrices [2], each beat per channel has about 410 matrix computations involving multiplications. All the 12 to 15 channels have to compute concurrently, acquiring digitized time series of ECG on all the channels, for applying same algorithm on multiple data from different channels. Thus arises, requirement of evolving general parallel architecture to embed various wavelet based algorithms of ECG Analysis [3] and Perception for Deviation Detection required for various diagnostic purposes.

2. PROPOSED METHOD

2.1 Wavelet Transform Principles

Unlike Short Time Fourier Transforms (STFT) meant for stationary waves, Wavelet Transforms provide both time and frequency resolution of interest in processing wavelets. It is possible to have temporal and frequency spectral information

in the form of coefficients, simultaneously, so it is suited for determining characteristic points of non stationary and fast transient signals, such as ECG signals. This characteristic will be suitableness to recognize the ECG signal starting with noise and interferences. The wavelet system decomposes a time variant signal into a few components having different scales or resolutions. An appropriate time and frequency limited wavelet will be picked as the mother wavelet. By scaling and moving the mother wavelet [4] a family of functions known as daughter wavelets may be produced. For little quality of the scale factor, wavelet will be constructed in the time domain and provides for majority of the data regarding fine subtle elements about signals. In this manner a worldwide see of the sign is acquired by the scale component expansive quality [5] The wavelet change of a time signal at whatever scale will be the convolution of the signal and a time-scaled daughter wavelet.

Essentially, there are two types of wavelet decompositions: continuous wavelet transforms and the non redundant ones such as orthogonal, semi-orthogonal, or bi-orthogonal wavelet bases [6]. The first type is preferable for feature extraction because it provides for a description that is truly shift-invariant. The second type is preferable for data reduction, or when the orthogonality of the representation is an important factor. However, the choice between these types of decompositions has to take into account computational considerations, too. A decomposition in terms of wavelet bases using Mallat fast algorithm is typically orders of magnitude faster than a redundant analysis, even if the fastest available algorithms are used [3], [4] in image domain applications.

As the aim of this paper is to evolve a general parallel architecture for suggesting, fast parallelized algorithm based on non redundant wavelet decompositions is important. To calculate the best wavelet function to be used, the ECG signal properties have been deliberated, for example, the shape and the time localization of occasions. The temporal signal shape will be a critical parameter, thus orthogonal wavelets are unsatisfactory will a chance to be utilized. Indeed they would incapable to give acceptable symmetry in the time domain and they present non-linear phase shift. The signal shape is conserved whether the phase shift is linear. Consequently the wavelet to be embraced must a chance to be a symmetrical function [7]. Spline wavelets have properties fulfilling the past prerequisites.

The higher order spline wavelet results, in very close to corresponding segment representation of ECG wave, which is always desirable. Higher order spline wavelet has larger coefficient series or matrix leading to more computational time consumption. Therefore, the cubic spline wavelet is assumed to have an order high enough for ECG application in order not to lose high frequency components required for deviation detection for diagnostic purpose. Traditional wavelet theory [6] and corresponding algorithms, consider decomposition suitable for single channel ECG that does not concurrently compute wavelet coefficient matrices 410 no.s per heart beat per channel, simultaneously acquiring all the 12 to 15 ECG channels, for deviation detection, to pinpoint or localize to a specific heart ailment, for on line diagnostic purposes. So, the novel computational techniques, such as parallel processing, concurrent programming evolving suitable architecture is required, choosing from the architectural research space. The Mallat algorithms for parallelized filter bank design have been used in [7]. The algorithm generates a set of parallelized perfect-reconstruction filter banks for an arbitrary number of end-nodes of a traditional tree structure [8]. This parallel architectural design evolution review, is in continuation to the work on Wavelet Transforms researched for Deviation detection of frequency domain ECG Signals, digitized as time series [9] and are considered for embedding in the general architecture evolved for usage of such Wavelet Transform based computations, for further future diagnostic research purposes.

2.2 Parallel Architecture For ECG Digital Signal Processing

In ECG there are 12 Channels for acquisition, Lead I, Lead II, Lead III, aVR, aVL, aVF, V_1, V_2, V_3, V_4,V_5,V_6. If, these 12 Channels have to be digitized and subjected to Wavelet Transforms concurrently, acquiring simultaneously, parallel Wavelet Transforms have to be computed, in on-line ECG systems for monitoring and detection purposes. In the algorithm [10], the heart beat period is approximately segmented into 410 splines and the corresponding coefficient matrices for each spline have to be computed per beat for all the channels, approximately in less than a second period at a heartbeat of around 72 beats per second. Such continuous monitoring of ECG for deviation analysis need Parallel Architectures, to extract ECG features such as „P", „QRS","T","U" waves and detect deviations in these waves. Unlike in general parallel configuration, 12 Analog to Digital Converters (ADC) also need to be incorporated in the Architectural Design.

2.3 Single Instruction Multiple Data (SIMD)

There are mainly four parallel configurations available in the parallel processing domain: they are Single Instruction Single Data (SISD), as in figure 1 Single Instruction Multiple Data (SIMD)[10], Multiple Instruction Single Data (MISD), Multiple Instruction Multiple Data (MIMD). In the present ECG systems, there are 12 Channels; where as in the future ECG systems under research, 15 Channels are likely, for concurrent and simultaneous processing. In addition to keeping a Processing Element (PE) per channel a PE is also required for front end jobs.

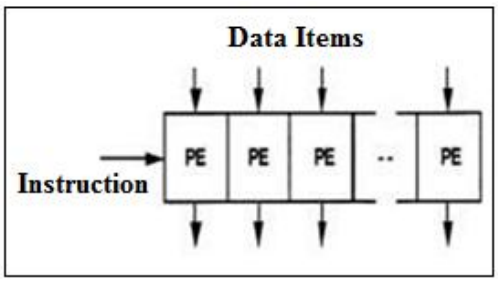

Figure 1: SIMD (Single Instruction Multiple Data)

Analog Signal from every channel is converted to a time series, using around 12 to 15 Analog to Digital Converters at the pre stage of the parallel processing. ECG processing is by Wavelet Transforms, executed by Parallel Processing

Elements (PEs) in the architecture. The PEs need to concurrently execute, the same instruction in the case of M/c code concurrently on Multiple Data obtained via ADCs or M/c code equivalent to same statement in the case of Parallel Pascal or „C". Multiple Data from multiple channels appear to the same processor instructions, in all the Wavelet Transform PEs.

So, out of all the general parallel processing configurations, Single Instruction Multiple Data (SIMD) shown in Figure 1 suite the ECG processing application for deviation detection based on Wavelet Transformations, for on line diagnostic purpose.

2.3 Parameters of Trade off for Parallel Processing Architecture Design

a. Principle of Operation
b. Processing Array
c. Processing Element (PE)Design
d. Parallelism Vs Machine Parallelism
e. Input/output Design for Arrays
f. Parallel languages available for the arrays

Based on the above design logic, the principle of operation chosen is SIMD: Single Instruction (of ECG Processing) Multiple Data (Operated on multiple Digitized data from 12 or 15 ECG Channels). The chosen ECG Processor, i.e SIMD processor has a single Control Unit, reading instructions pointed to by a single ECG Program Counter (PC), decoding them and sending control signals to the Processing Elements (PEs) of the ECG Processor Array. Data are to be supplied to and derived from the Processing Elements (PEs) by a memory with as many data paths as PEs as shown in figure 2. So, after the trade off, two dimensional mesh connected Processing Array configuration with 16 ECG PEs for embedding DSP wavelet transform software are chosen as shown in the Figure 2 below

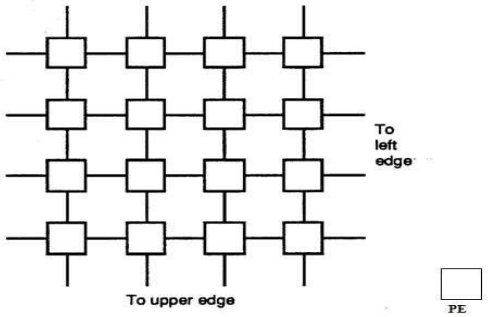

Figure 2: 16 PEs Parallel Array configuration for ECG Digital Signal Processing

In the above parallel configuration lower edge is connected to upper edge and left edge is connected to right edge. In the tradeoff between processing capacity and parallelism, it is going for less processing power for ECG processing and more size of the array, i.e how one to one PEs are chosen as per number of channels and a front end processor, i.e 16 no.s of PEs, considering maximum number of channels possible in ECG. In ECG processing, as the incoming channels provide, time series, after digitization (i.e after ADC stage), the natural choice in the design architecture is Bit-Serial Processors as PEs with more parallelism in the array.

2.4 Processing Element Design

The Processing Element design has a trade off, between embedding a 32 Bit Floating Point processor[10][11] for matrix computations involved in Wavelet Transformations or Bit Serial Multiplier, depending on parallel language support and VLSI real estate and cost. Bit Serial Multiplier occupies less design space and less costly. Signal processing through Wavelet Transformations need faster multiplication units. So, enhanced Bit Serial PEs with Bit Serial Multiplication units, suite ECG Processing architecture. Simple Bit- Serial processor has the drawback of growth of multiplication time quadratic ally with the data width. The configuration chosen for the design is shown below in Figure 3, does the bit-serial multiplication in no more than, what is needed to read the operands bit by bit.

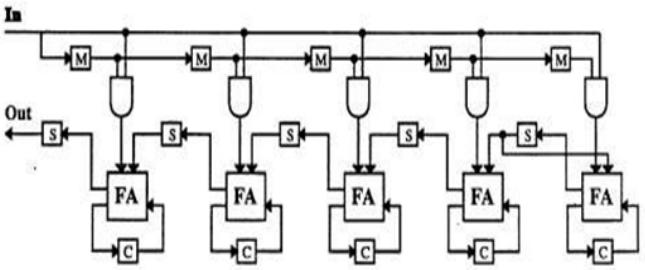

Figure 3: Bit Serial multiplier for PEs of ECG Processing

This method of multiplication is based on a carry-save adder technique that requires as many full adders as the data width. In the multiplier of each ECG Processing Element, there will be 32 Full adders to make 32 Bit multiplication operations. It operates by first shifting in, the multiplicands, most significant bit first, into the array of „M" flip-flops. The bits of the multiplier are then successively applied to the input, least significant bit first and the product bits appear at the output, also least significant bit first.

2.5 Input / Output Design for SIMD Array

In order to obtain a well balanced architecture, the design of the I/O system is as important as the design of Processing Elements (PEs) and array topology. Input/output design is discussed below in terms of different classes of data formats required.

Conventional format: ECG Signal Data processing is by using the traditional data format used in conventional computers

Processing format: Bit-Plane format is the processing data format of arrays with Bit-Serial PE Application format: It is the format of ECG Data

The Design of I/O system is such that to serve as an interface between the different formats indicated above at various stages of processing. In real time applications, with processor arrays directly connected to input and output devices, the interface between the application data format and the processing format is most important. Transfer between word at a time of the front end processor and the processing array must be efficient. The chosen design for I/O.

A set of 8-Bit I/O Registers (shift registers) is connected to the Memory Array, one register per memory word. The I/O

registers can be read or written from the Front-End Processor, in the conventional word at a time format. A data input process can be divided into two phases: one to fill the I/O registers from the Front-End or I/O Processor, one to shift the contents portion of the I/O registers and in to any field of the Memory Array. The first phase needs one write cycle of the Front-End or I/O Processor to transfer 8 bits, the second phase requires 8 Memory Array write cycles in each of which an entire bit-slice is transferred. In the case of inter Processor Element (PE) communication, the same I/O design scheme without addressing of the I/O registers, data is shifted in and out of the registers or Bit-Serial communication, which also exists in the configuration or the architecture.

3. RESULT & ANLAYSIS

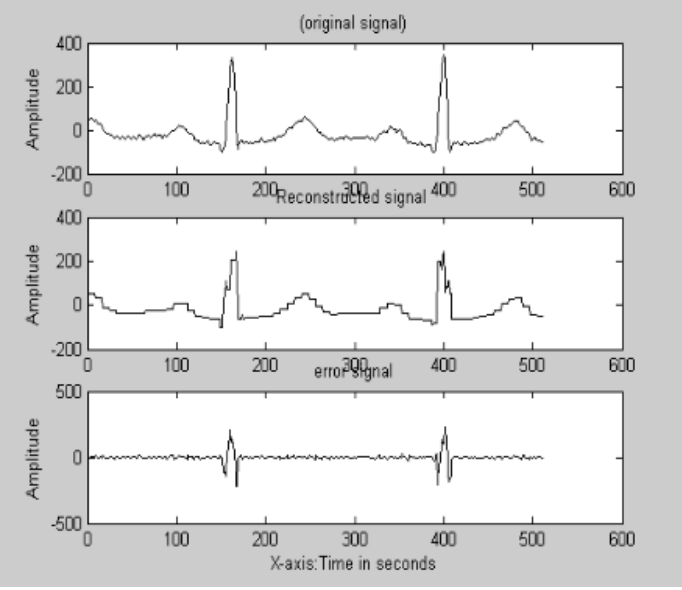

Figure 4: Compression using wavelet with CR = 10:1 and PRD = 1.02

3.1 Wavelet Analysis Methodology

As in figure 4 is intended for evolving the above suggested architecture, the following illustrative steps of part of the algorithm are briefly indicated here, from our publication on Wavelet Analysis methodology [3], to indicate embedded Wavelet Transforms for such general parallel architectures.

Inverse of a Matrix A = Adj A/det A, Adj A = $[\text{Cofactor A}]^T$

In the Wavelet Analysis methodology of [3] the Transpose of Cofactor Matrix, to obtain inverse of 410 matrices required, for further computations of wavelet coefficient matrix is computed in two steps as indicated below, where va[0] to va[3], vtmp[0] to vtmp[3] and vaT[0] to vaT[3] are respective illustrative variables.

Parallel C and Parallel Pascal are available for some of the architectural space or configurations, for developing parallel algorithms, wherever task scheduling is required for configuration deviations, for design and cost trade off at the time of implementation, front end processor is expected to play the scheduling role, which appears to be optimal solution for ECG parallel processing architecture.

4. CONCLUSION

In this review article, a complete general parallel architecture to embed algorithms of Wavelet Transforms for deviation detection of ECG is evolved, for online medical applications, in continuation to our research work, done on spline based Wavelet Transform [3], for diagnostic purpose. The suggested architecture, supports in evolving various Wavelet Transform based digital signal processing algorithms for online ECG diagnostics, to associate, deviations in ECG electrical waveform with deterioration in the specific anatomical function of heart, as research proceeds, in this diagnostic method. For example inverted T waveform of ECG indicates ischemia.

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