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Robust and Power-Aware Design of CNFET-Based XOR Circuit at 16-nm Technology Node

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Abstract— Motivations of CMOS technology scaling are higher speed of operation, benefit of integration density and lower power dissipation. CMOS technology has crossed many hurdles over the past four decades. The aggressive technology scaling is causing device parameter variations, which is more severe than earlier. This paper carries out variability analysis of various popular exclusive-OR circuits at the transistor level in terms average power and power-delay product (PDP) at 16-nm technology node. A simulation framework, consisted of the gate under test loaded with two nominal copies of the corresponding XOR gate at both the ends – input and output, is used for the analysis. The aim of this work is to determine the circuit with least variability of PDP. Finally, it realizes the best XOR circuit using an emerging device namely carbon nanotube field effect transistor (CNFET). At nominal supply voltage of V_{DD} = 0.7 V, the proposed CNFET based realization of XOR circuit offers 1.63 × improvement in PDP variability and 6.15 × improvement in PDP compared to its CMOS counterpart.

Keywords— carbon nanotube field effect transistor (CNFET), low-power, power delay product (PDP), propagation delay, robust, variability.

INTRODUCTION

An exclusive-OR gate acts as a buffer when one of its inputs is low; on the other hand, it acts as an inverter when one of its inputs is high. Therefore, XOR gate is used as controlled inverter. XOR gate represents “odd function”.

XOR gate finds its application in various logic circuits such as shift register, parity generator/checker for error detection/correction, gray to binary and binary to gray code converter [1]. XOR gate is the integral component of arithmetic circuits such as full adder and multiplier. It is also extensively used in circuits such as compressors, comparators and phase detector [2].

Circuits like full adders are more critical as they play an important role for many useful operations like multiplication and division. They are a part of the critical path and thereby influence the overall performance of the entire system.

Desired feature for the design of a XOR cell is to have a small number of transistors to implement it and low power dissipation. NAND/NOR functions have a compact implementation in the well-established CMOS technology [3]. However, XOR circuit has various realizations. For instance, a direct realization of an XOR function using static CMOS logic requires 12 MOSFETs [4]. Circuits based on pass transistors can be a solution to this problem, but it has its own limitation such as low output level for certain input patter due to threshold voltage drop. XOR circuit being the basic building block of many useful circuits, proper selection of these circuits can enhance the performance of larger number of circuits that they are part of. Therefore, it is extremely desirable to select XOR circuit with optimum design metrics. What is meant by optimum design is to avoid degradation of output level, have lower propagation delay (t_p) and power-delay product (PDP) [5].

This paper makes following contributions:

It analyzes 5 different XOR circuits in terms of various design metrics such as average power (PWR), PDP and their variabilities.

- Design metrics like PWR and PDP are estimated with Monte Carlo simulation using simulation framework loaded with two nominal copies of the corresponding XOR gates at input and output.
- The XOR circuit with least variability of PWR and PDP is realized with carbon nanotube field effect transistors (CNFETs).

To verify the proposed design, extensive simulations on HSPICE using 16-nm PTM (developed by the Nanoscale Integration and Modeling (NIMO) Group at Arizona State University (ASU) [6] are carried out.

The remainder of this paper is organized as follows. Various XOR designs are briefly reviewed in Section II. Section III compares XOR circuits at nominal V_{DD} of 0.7 V. Variability analysis results are also discussed and compared in Section III. Implementation of best XOR circuit using CNFETs is brought up in Section IV. Finally, the conclusion of the paper appears in Section V.

ANALYSIS OF VARIOUS XOR GATE

XOR circuit presented in [5] (Fig. 1) is based on GDI technique. This technique maintains low complexity of logical design and allows the reduced power consumption, propagation delay and area [7]. However, GDI based XOR (GDI-XOR) circuit gives a bad 1 for ‘10’ (AB = 10) input

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pattern. At '10' input condition, P1 turns ON unlike N1, at the same time P2 turns OFF but N2 conducts, this makes XOR output connected to V_{DD} via N2, which leads to a bad 1 due to V_{tn2} drop across N2. Moreover, its voltage level remains V_{tp2} above the ground level for '00' input pattern as P2 stops conducting when XOR output falls just below V_{tp2}.

XOR circuit shown in Fig. 2 has pass transistor logic (PTL) with output buffer. Here transistors act as switches to pass logic levels between nodes of the circuit, rather than switches connected directly to supply voltages. Therefore, this can reduce the number of active devices, but, at the same time, it has a disadvantage that the difference of the voltage between high and low logic levels decreases at each stage. PTL XOR cell [1] provides good output voltage levels for all input pattern, except for the '11' input pattern. For '11' input pattern, P1 and P2 turn OFF while N1 and N2 turn ON. The node '1' does not rise up to V_{DD} due to V_{tn2} (or V_{tn1}) drop. This low node 1 voltage weakly drives the output inverter, resulting in bad zero at XOR output.

7T XOR circuit [8] shown in Fig. 3 comes up with a solution of threshold voltage loss and results in a full voltage swing. In other words, unlike 6T XOR circuits its internal nodes do have a full voltage swing, thereby showing a perfect response for all possible input patterns.

Low power XOR (LP-XOR) circuit shown in (Fig. 4) is based on optimized implementation for XOR function [9]. It employs high functionality of PTL style. Though the circuit has a non-full voltage swing at the output node but is characterized by its low power consumption. Its XOR circuit gives a bad 0 for '00' input pattern. For '00' inputs P1 and P2 turn ON, and N1 and N2 turn OFF, thereby disconnecting ground form output and its voltage level remains V_{tp2} (or V_{tp1}) above the ground level because P2 (or P1) stops conducting when XOR output falls just below V_{tp2} (or V_{tp1}).

CMOS inverter XOR (INV-XOR) circuit illustrated in Fig. 5 consists of inverter which restores signal level and improves driving capability [10]. However, it has the drawback of extra power consumption. The XOR circuit yields a bad 0 and a bad 1 for '00' and '10' input pattern respectively. For '00' inputs P1 and P2 turn ON unlike N1 and N2. XOR output drops down to a voltage V_{tp2} above the ground, because below V_{tp2}, P2 stops conducting, thereby giving a bad 0. For '10' input condition, XOR output gets connected to V_{DD} via N2 and P1, which leads to a bad 1 due to V_{tn2} drop across N2.

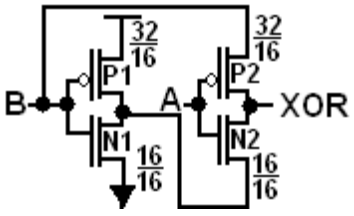

Fig 1: GDI-XOR Cell [5]

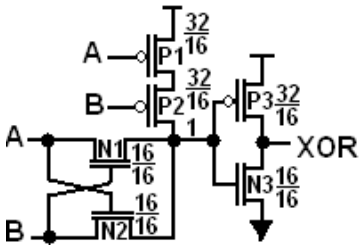

Fig 2: PTL XOR Cell [1]

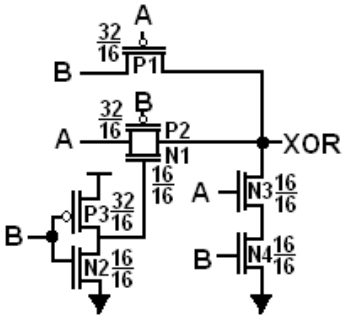

Fig 3: 7T XOR Circuit [8]

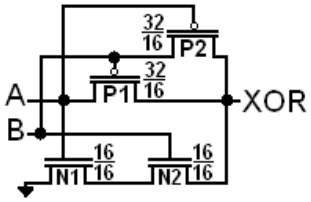

Fig 4: LP- XOR circuit [9]

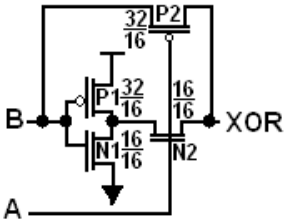

Fig 5: INV- XOR circuit [10]

SIMULATION RESULTS AND DISCUSSION

A. Estimation of Propagation Delay, Power Dissipation and Power-Delay Product at Nominal Supply Voltage

The circuits discussed above were successfully simulated on HSPICE using 16-nm technology node at nominal supply voltage of 0.7 V. Simulation results depicting the values of t_P, PWR, and PDP are reported in Table 1. As can be observed from Table 1, LP-XOR exhibits lowest PDP showing its superiority compared to other circuits.

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TABLE 1: Comparison of Propagation Delay, Power Dissipation and Power-Delay Product at Nominal V_{DD} of 0.7 V

XOR Circuit	t_p (ns)	PWR (nW)	PDP (aJ)
GDI XOR	2.2849	9.5669	21.860
PTL XOR	2.3106	156.87	362.45
7T XOR	2.3016	10.275	23.649
LP-XOR	2.2938	0.6604	1.5148
INV- XNOR	2.2849	9.5669	21.860

B. Variability Analysys of XOR circuits

The focus of this work is on the challenges faced in designing logic circuit in nanometer regime, where variations occur due to process and environmental parameters such as operating voltage and temperature. The root cause of variations is scaling. The problem of variability (defined as standard deviation (σ) to mean (μ) ratio of a design metric) becomes more severe with greater miniaturization and hence, it is imperative that this problem be addressed [11].

Design metrics such as of PWR and PDP are estimated with Monte Carlo simulation using simulation framework shown in Fig. 6. To make the input and output of the XOR gate under test realistic it is loaded with two nominal copies of the relevant XOR gates at both the ends – input and output.

In this analysis, parameters for CMOS circuits such as, channel length (L_{ch}), channel width (W), channel doping concentration ($NDEP$), oxide thickness (t_{ox}), threshold voltage (V_t) are assumed to have independent Gaussian distributions with 3σ variation of 10% [12]. Design metrics of CNFET circuits was estimated by varying L_{ch}, LSS/LDD (length of doped CNT source/drain-side extension region), E_{fo} (S/D n+/p+ doped CNT Fermi-level), t_{ox} and $Pitch$ (distance between the centers of two adjacent CNTs) by ±10%.

As per ITRS 2009, expected variation in V_{DD} is ±10% in future technology generations [12]. Hence, most of the design metrics are estimated by varying the supply voltage by ±10% around the nominal V_{DD} of 0.7 V. The sample size of 2000 ensures a lower than 4% inaccuracy in the estimation of standard deviation [13]. Design metrics in this work are estimated with 5000 sample size to achieve even higher accuracy.

In digital electronics, PDP is a figure of merit correlated with the energy efficiency of a logic gate or logic family. It is the product of average power consumption (PWR) and propagation delay (t_P). It has the dimension of energy, and measures the energy consumed per switching event. Lower the value of PDP, better is the design.

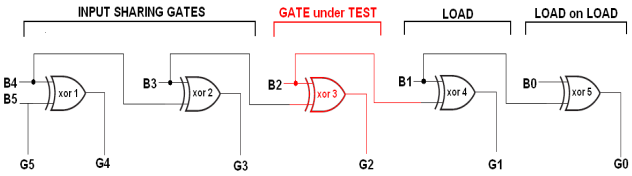

Fig 6: Simulation framework for estimation of variability analysis.

TABLE 2: Variability Comparison of Power Dissipation

V_{DD} (mV)	σ/μ GDI-XOR	σ/μ PTL-XOR	σ/μ 7T-XOR	σ/μ LP-XOR	σ/μ INV-XOR
630	2.93	0.77	3.01	0.15	2.93
665	2.75	0.77	2.84	0.18	2.75
700	2.57	0.75	2.64	0.23	2.57
735	2.39	0.73	2.44	0.25	2.39
770	2.22	0.71	2.25	0.24	2.22

TABLE 3: Variability Comparison of Power-Delay Product

V_{DD} (mV)	σ/μ GDI-XOR	σ/μ PTL-XOR	σ/μ 7T-XOR	σ/μ LP-XOR	σ/μ INV-XOR
630	2.95	0.79	3.03	0.15	2.95
665	2.77	0.79	2.84	0.18	2.77
700	2.59	0.77	2.64	0.23	2.59
735	2.40	0.75	2.44	0.25	2.40
770	2.23	0.72	2.25	0.24	2.23

The variability of power and PDP of all the XOR gates are estimated scaling the supply voltage (V_{DD}) from 770 mV down to 630 mV (nominal V_{DD} ± 10%). It is observed from the simulation results tabulated in Tables 2 and 3, that LP-XOR exhibits narrower spread in PWR as well as PDP at all considered V_{DD} as compared to other four XOR gates. Therefore, LP-XOR based circuit will be robust compared to the circuit based on other XOR gates.

NEED FOR EMERGING TECHNOLOGY

Recent technological development such as CNFET and FinFET are the promising technologies of choice to replace traditional MOSFET in the nanoscale design [12]. Out of the nanoelectronic devices researched till date, CNFET seems to have the brightest prospect due to its better electronic characteristics. Speed enhancement due to scaling down to 16-nm and 10-nm technology node has given the impetus to its use.

A. CNFET Structure and its Characteristics

CNFET consists of carbon nanotube (CNT). CNT is basically a long, thin allotropic carbon tube which provides a single path between source and drain. CNTs are sheets of graphite rolled into hollow cylinders of diameters varying from 0.4 nm to 4 nm [14]. CNTs exhibit unique electrical properties and extraordinary strength. CNTs derive their name from their size, as the diameter of a nanotube is on the order of a few nanometers, while they can be up to 18 centimeters in length (as of 2010) [15].

Literature survey shows that a CNFET circuit with one to ten CNTs per device is about two to ten times faster compared with CMOS circuits [16], [17]. Fig. 7 illustrates a typical structure of a CNFET with multiple CNTs. CNTs are placed on substrate having dielectric constant of K_{sub} = 4. Doping variation along the length of CNT shows that the channel region of CNTs is un-doped, and the other regions of CNTs are heavily doped. High-k (Hi-k) material (HfO_2) having

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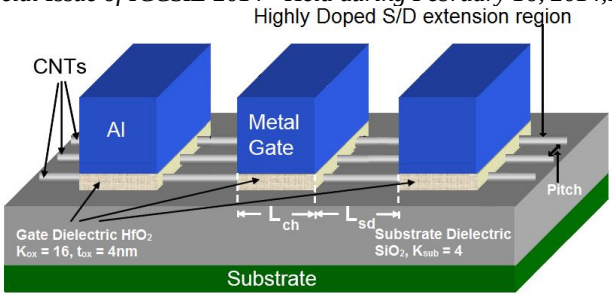

Fig 7: A typical CNFET structure with multiple CNTs [17]

TABLE 4: Device and Technology Parameters for CNFET

Parameter	Description	Value
L_{ch}	Physical channel length	16 nm
W_{mg}	The width of metal gate (sub_pitch)	6.4 nm
t_{ox}	The thichness of high-k top gate dielectric material (planar gate)	4 nm
K_{ox}	Dielectric constant of high-k gate oxide	16
(n_1, n_2)	Chirality of the tube	(19,0)
n_CNT	Number of tube per device	4

dielectric constant of (K_{ox}) 16 and thickness (t_{ox}) of 4 nm is used as insulating material in the channel. The effective width of the multi-tubed CNFET (W_g) is defined as W_g = Pitch×(N_{CNT})+D_{CNT}, where Pitch is the distance between centre of two adjacent tubes (see Fig. 7), n_CNT is the number of tubes and DCNT is the diameter of tube. Therefore, the aspect ratio (W_g/L_{ch}) of the CNFET used in this work is 1.185 (16nm/13.5059nm), as D_{CNT} for n_1=19 and n_2=0 is calculated to be 1.5059nm. Other important device and technology parameters related to CNFET are tabulated in Table 4.

A single-walled CNT (SWCNT) can work differently depending on its chirality (n_1, n_2) – the direction in which the single atomic layer of graphite is rolled up to form a seamless cylinder. The CNT acts as metal if $n_1 = n_2$ or $n_1 - n_2 = 3i$, where i is an integer. Otherwise, CNT works as semiconductor. The D_{CNT} (diameter of CNT) is calculated using chirality vector (n_1, n_2) as

$$D_{CNT} = \frac{a}{\pi}\sqrt{n_1^2 + n_2^2 + n_1 n_2} \qquad (1)$$

where a = 2.49Å, is the CNT atomic distance. The variations in diameter of CNT (DCNT) is achieved by varying its chirality vector (n_1) (see Fig. 8). This in turn helps in estimating propagation delay (t_P) by varying D_{CNT}. The estimated t_p versus diameter is ploted in Fig. 9. The t_P decreases with increase in D_{CNT} (see Fig. 9). This is because the E_g (energy gap) decreases with increase in D_{CNT} (2). This enables large number of charge carriers to overcome the energy barrier, resulting in higher current flow and lower propagation delay. The relationship between E_g and D_{CNT} is given in (2)

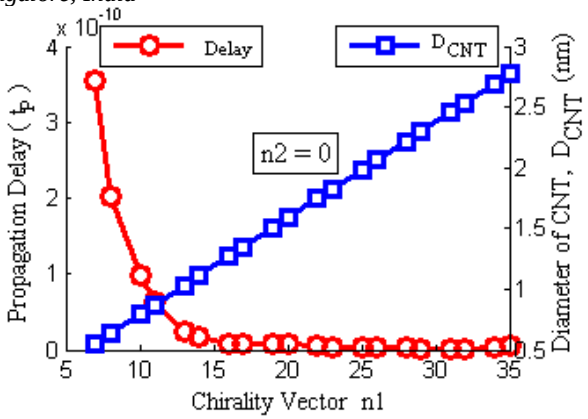

Fig 8: CNT diameter and Delay variations with Chirality Vector n_1

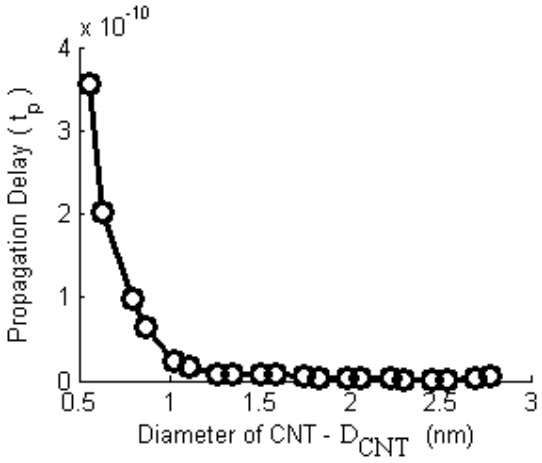

Fig 9: Variation of propagation delay with CNT diameter

$$E_g = \frac{0.84eV}{D_{CNT}} \qquad (2)$$

where "e" is electronic charge.

B. *Variability Analysis*

Leakage current, high field effect, short channel effect and lithographic limit problems associated MOSFET are largely taken care of in CNFET [18]. The robust circuit emerged out in the analysis in Section IV is the LP-XOR gate, which is realized with CNFET (see Fig. 10), its PDP and PDP variability are compared with that of its CMOS counterpart. The proposed CNFET-based design is simulated in HSPICE using the experimentally validated CNFET model [19]–[22]. The estimated results of PDP and its variability are reported in Tables 5 and 6. The same are also plotted in Fig. 11 for making the comparison easier.

The proposed CNFET based LP-XOR circuit (see Fig. 10) exhibits lower PDP at all considered V_{DD} compared to MOSFET based LP-XOR circuit. In particular, it shows 6.15×

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lower PDP compared with its CMOS counterpart at nominal

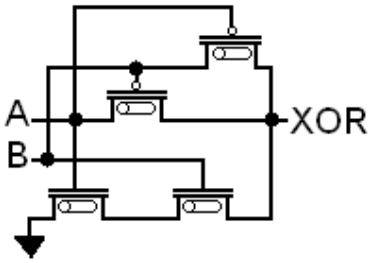

Fig 10: Proposed CNFET based LP-XOR gate.

TABLE 5: Power-Delay Product Comparison Between CNFET Based LP-XOR and MOSFET based LP-XOR

V_{DD} (mV)	MOSFET based LP-XOR (aJ)	CNFET based LP-XOR (aJ)
630	2.2467	0.33432
665	2.3419	0.33267
700	2.5148 (6.15)	0.40868
735	2.5357	0.43908
770	3.2742	0.46208

TABLE 6: Variability Comparison of Power-Delay Product Between CNFET Based LP-XOR and MOSFET based LP-XOR

V_{DD} (mV)	MOSFET based LP-XOR	CNFET based LP-XOR
630	0.154	0.109
665	0.180	0.121
700	0.230 (1.63)	0.141
735	0.248	0.155
770	0.244	0.160

V_{DD} of 0.7 V (normalized value is shown within bracket). The proposed design exhibits its robustness by showing narrower spread in PDP at all considered V_{DD}. In particular, it offers 1.63× improvement in PDP variability at nominal voltage of V_{DD} = 0.7 V (normalized value is shown within bracket). In the CNFET, electrons are confined within the narrow nanotube, which has quasi 1-D structure. CNFET utilizes ballistic transport property of CNT. Ballistic transport means that the mean free path for a charge carrier is longer than the device dimensions and hence charge carriers do not collide during its travel from source to drain due to longer mean free path. This leads to higher mobility of carriers in CNFET than in MOSFET. The higher electron mobility compared to MOSFET offers higher drive current reducing propagation delay and hence PDP. The likely causes of reduction of PDP variability are attributed to the fact that the gate width in CNFET is not the effective channel width of the transistor. The channel width actually depends only on the tube diameter and the number of tubes under the gate. Hence, unlike MOSFET, variation of the conventional channel width does not affect the drive current. Only the CNT diameter has strong impact on its drive current, while other process parameter variations have very small impact. The impact of DIBL (drain-induced barrier lowering) or SCE (short-channel effect) is pronounced on drive current of MOSFET compared to that of CNFET.

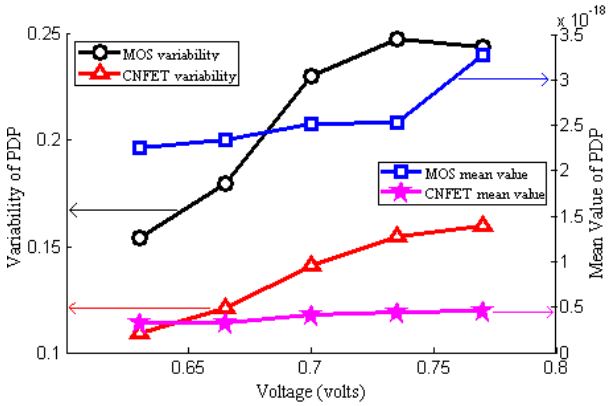

Fig 11: PDP and its variability comparision.

CONCLUSION

This paper successfully investigated various XOR circuits in terms of design metrics like power and PDP. LP-XOR circuit is found to offer least variability of PWR and PDP. The same is realized with CNFET. The proposed CNFET realization exhibits lower PDP compared to it's CMOS counterpart. This work also carries out variability analysis of the proposed circuit. CNFET implementation shows its robustness against PVT variation. Therefore, proposed CNFET implementation is an attractive choice to achieve higher immunity against variations, which is inherent in nanoscale circuits.

REFERENCES

[1] Shinichi Nishizawa, Tohru Ishihara, and Hidetoshi Onodera,"Analysis and comparison of XOR cell structures for low voltage circuit design" in Quality Electronic Design (ISQED), 2013 14th International Symposium, pp. 703-708, Mar 2013.

[2] Rajeev Kumar and Vimal Kant Pandey, "A new 5-transistor XOR-XNOR circuit based on the pass transistor logic" in Information and Communication Technologies (WICT), 2011 World Congress, pp. 667-671, Dec 2011.

[3] Luca Amar´u, Pierre-Emmanuel Gaillardon and Giovanni De Micheli, "MIXSyn: An efficient logic synthesis methodology for mixed XOR-AND/OR dominated circuits" in Design Automation Conference (ASP-DAC), 2013 18th Asia and South Pacific, pp. 133-138, Jan 2013.

[4] M. Vesterbacka, "A new six transistor CMOS XOR circuit with complementary output" in Circuit and Systems 1999, 42nd Midwest Symposium., vol 2, pp.796-799, Aug 1999.

[5] Aminul Islam, A. Imran and Mohd. Hasan, "Variability analysis and FinFET based design of XOR and XNOR circuit" in Computer and Communication Technology (ICCCT), 2011 2nd International Conf, pp. 239-235, Sept 2011.

[6] Nanoscale Integration and Modeling (NIMO) Group, Arizona State University (ASU). [Online]. Available: http://ptm.asu.edu/.

[7] Arkadiy Morgenshtein, Alexander Fish, and Israel A. Wagner, "Gate-diffusion input (GDI): a power efficient method for digital combinatorial circuits" IEEE Trans., vol. 10, October 2002, pp. 566-581.

[8] Hanho Lee and Gerald E. Sobelman, "New low voltage circuits for XOR and XNOR", Proc. IEEE, pp.225-229, Apr 1997.

[9] Sumeer Goel, Mohammed A. Elgamel, Magdy A. Bayoumi, and Yasser Hanafy, "Design methodologies for high performance noise tolerant XOR–XNOR circuits" IEEE Trans. vol 53, pp. 867-878, Apr 2006.

[10] Sumeer Goel, Mohamed A. Elgamel and Magdy A. Bayoumi, "Novel design methodology for high performance XOR-XNOR circuit design" in Integrated Circuits and Systems Design, 2003. SBCCI 2003, pp. 71-76, Sept 2003.

[11] Aminul Islam and Mohd. Hasan, "Leakage charaterization of 10T SRAM cell" IEEE Trans. Electron Devices, vol 59, no. 3, pp. 631-638, Mar 2012.

[12] http://www.itrs.net/Links/2009ITRS/Home2009.htm

[13] M. Alioto, G. Palumbo, and M. Pennisi, "Understanding the effect ofprocess variations on the delay static and domino logic," IEEE Trans.Very Large Scale Integr. (VLSI) Syst., vol. 18, pp. 697–710, May 2010.

[14] A. Kumar, S. Prasad and A. Islam, "Realization and optimization of CNFET based operational amplifier at 32-nm technology node" in proc of: International Conclave 2013 "Innovations in Engineering & Management"(ICIEM 2013), Feb 2013.

[15] X. Wang, et al., "Fabrication of ultralong and electrically uniform single-walled carbon nanotubes on clean substrates," Nano Lett., vol. 9, pp. 3137–3141, Aug. 2009.

[16] J. Deng, and H.-S. P. Wong, "A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application - part I: model of the intrinsic channel region," IEEE Trans. Electron Devices, vol. 54, pp. 3186-3194, Dec. 2007

[17] J. Deng, and H.-S. P. Wong, "A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application - part II: full device model and circuit performance benchmarking," IEEE Trans. Electron Devices, vol. 54, pp. 3195-3205, Dec. 2007.

[18] J. Deng, "Device modeling and circuit performance evaluation for nanoscale devices: silicon technology beyond 45 nm node and carbon nanotube field effect transistors," Ph.D. dissertation, Dept. Elect. Eng., Stanford Univ., Cambridge, MA, 2007.

[19] Stanford University CNFET Model, (2008). [Online]. Available: http://nano.stanford.edu/model.php?id=23.

[20] J. Deng, and H.-S. P. Wong, "A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application - part I: model of the intrinsic channel region," IEEE Trans. Electron Devices, vol. 54, pp. 3186-3194, Dec. 2007.

[21] J. Deng, and H.-S. P. Wong, "A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application - part II: full device model and circuit performance benchmarking," IEEE Trans. Electron Devices, vol. 54, pp. 3195-3205, Dec. 2007.

[22] Farad Ali Usmani, and Mohammad Hasan, "Carbon nanotube field effect trasistors for high performance analog application: an optimum design approach," in Microelectronics Journal, vol. 41, pp. 395-402, July 2010.