ISSN
Volume 1, No.1, August- September 2012
International Journal of Wireless Communications and Networking Technologies
Available Online at http://warse.org/pdfs/ijwcnt07112012.pdf

An Efficient VLSI Design Approach to Reduce Static Power for Nano Scale CMOS VLSI Systems using Variable Body Biasing

V.V.S.R.K.K.Pavan BH[1], R.Vinay Kumar[2], M.Srihari [3],
[1]PG Student, Kakinada Institute of Engineering and Technology,Korangi, A.P., India. pjrece@gmail.com
[2]Assistant Professor, Kakinada Institute of Engineering and Technology, Korangi, Andhra Pradesh, India.
[3]Assistant Professor, Kakinada Institute of Engineering and Technology, Korangi, Andhra Pradesh, India.

ABSTRACT

The development of digital integrated circuits is challenged by higher power consumption. In CMOS integrated circuit design there is a trade-off between static power consumption and technology scaling. Recently, the power density has increased due to combination of higher clock speeds, greater functional integration, and smaller process geometries. As a result static power consumption is becoming more dominant. This is a challenge for the circuit designers. However, the designers do have a few methods which they can use to reduce this static power consumption. But all of these methods have some drawbacks. In order to achieve lower static power consumption, one has to sacrifice design area and circuit performance. In this paper, we propose a new method to reduce static power in the CMOS VLSI circuit using Variable Body Biasing technique without being penalized in area requirement and circuit performance.

Keywords: Dual Stack, Dual Vth, State Saving Technique, Static Power Reduction.

1. INTRODUCTION

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift where power dissipation has become as important a consideration as performance and area. Two Components determine the power consumption in a CMOS circuit;

Static power: Includes sub-threshold leakage, drain junction leakage and gate leakage due to tunneling. Among these, sub threshold leakage is the most prominent one. Dynamic power: Includes charging and discharging power and short circuit power. When technology feature size scales down, supply voltage and threshold voltage also scale down. Sub-threshold leakage power increases exponentially as threshold voltage decreases. Furthermore, the structure of the short channel device lowers the threshold voltage even lower. So it is becoming more and more important to reduce leakage power as well as dynamic power. There are several VLSI techniques for reducing leakage power. Each Technique provides an efficient way to reduce leakage power, but disadvantages of each technique limit its application. In this paper, we propose a novel dual stack technique that reduces not only leakage power but also dynamic power. We summarized and compared the previous techniques with our new approach.

2. PREVIOUS WORKS

Techniques for leakage power reduction can be grouped into two categories: state-preserving techniques; where circuit state is retained and state destructive techniques; where the current Boolean output value of the circuit might be lost. A state preserving technique has an advantage over a state destructive technique in that with a state-preserving technique the circuitry can resume operation at a point much later in time without having to somehow regenerate state. The most well-known traditional approach is the sleep approach. In the sleep approach, a "sleep" PMOS transistor is placed between Vdd and the pull-up network of a circuit and a "sleep" NMOS transistor is placed between the pull-down network and Gnd (Figure 1). These sleep transistors turn off the circuit by cutting off the power rails. The sleep transistors are turned on when the circuit is active and turned off when the circuit is idle. By cutting off the power source, this technique can reduce leakage power effectively. However, output will be floating after sleep mode, so the technique results in destruction of state plus a floating output voltage.

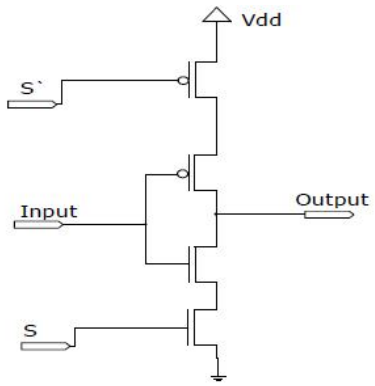


Figure 1:. Sleep method

A variation of the sleep approach, the zigzag approach, reduces wake-up overhead caused by sleep transistors by placement of alternating sleep transistors assuming a particular pre-selected input vector.

Another technique for leakage power reduction is the stack approach, which forces a stack effect by breaking down an existing transistor into two half size transistors. The divided transistors increase delay significantly and could limit the usefulness of the approach. The sleepy stack approach (Figure 2) combines the sleep and stack approaches. The sleepy stack technique divides existing transistors into two half size transistors like the stack approach. Then sleep transistors are added in parallel to one of the divided transistors. During sleep mode, sleep transistors are turned off and stacked transistors suppress leakage current while saving state. Each sleep transistor, placed in parallel to the one of the stacked transistors, reduces resistance of the path, so delay is decreased during active Mode. However, area penalty is a significant matter for this approach since every transistor is replaced by three transistors and since additional wires are added for S and S', which are sleep signals.

Another technique called Dual sleep approach (Figure 3) uses the advantage of using the two extra pull-up and two extra pull-down transistors in sleep mode either in OFF state or in ON state. Since the dual sleep portion can be made common to all logic circuitry, less number of transistors is needed to apply a certain logic circuit.

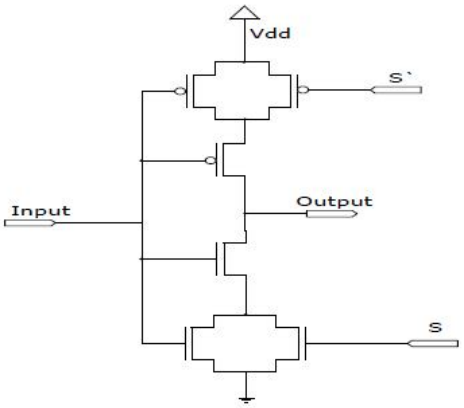


Figure 2: Sleepy stack

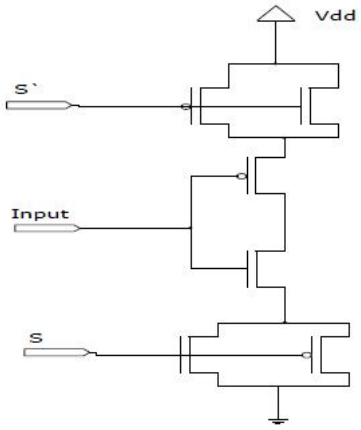


Figure 3: Dual sleep

3. NOVEL DUAL STACK APPROACH

In this section, the structure and operation of our novel low-leakage-power design is described. It is also compared with well-known previous approaches, i.e., the sleepy stack, dual sleep and sleep transistor methods. First we explain the circuit operation for a chain of 4 inverters (Figure 4) in sleep mode. In sleep mode, the sleep transistors are off, i.e. transistor N5 and P5 are off. We do so by making S=0 and hence S'=1. Now we see that the other 4 transistors P6, P7 and N6, N7 connect the main circuit with power rail. Here we use 2 pmos in the pull-down network and 2 nmos in the pullup network. The advantage is that nmos degrades the high logic level while pmos degrades the low logic level. Due to the body effect, they further decrease the voltage level. So, the pass transistors decreases the voltage applied across the main circuit.

As we know that static power is proportional to the voltage applied, with the reduced voltage the power decreases but we get the advantage of state retention. Another advantage is got during off mode if we increase the threshold voltage of N6, N7 and P6, P7. The transistors are held in reverse body bias. As a result their threshold is high. High threshold voltage causes low leakage current and hence low leakage power. If we use minimum size transistors, i.e. aspect ratio of 1, we again get low leakage power due to low leakage current. As a result of stacking, P6 and N6 have less drain voltage. So, the DIBL effect is less for them and they cause high barrier for leakage current. While in active mode i.e. S=1 and S'=0, both the sleep transistors (N5 and P5) and the parallel transistors (N6, N7 and P6, P7) are on. They work as transmission gate and the power connection is again established in uncorrupted way. Further they decrease the dynamic power.

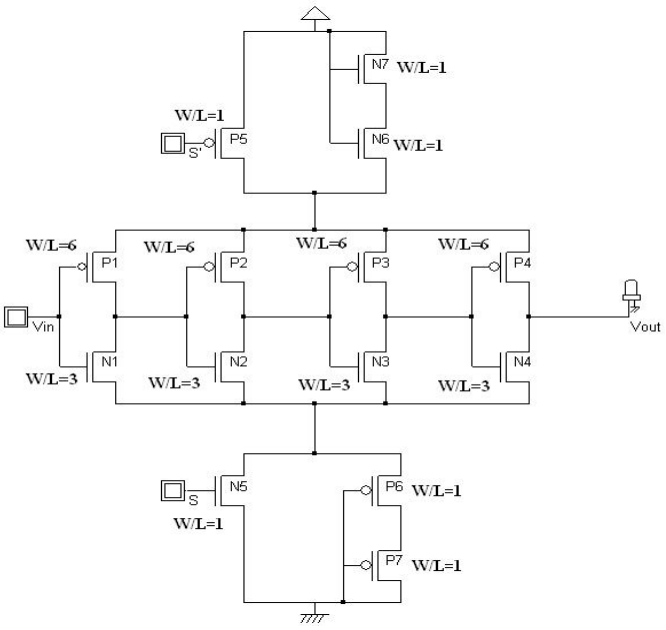


Figure 4: Dual stack approach (a chain of 4 inverters)

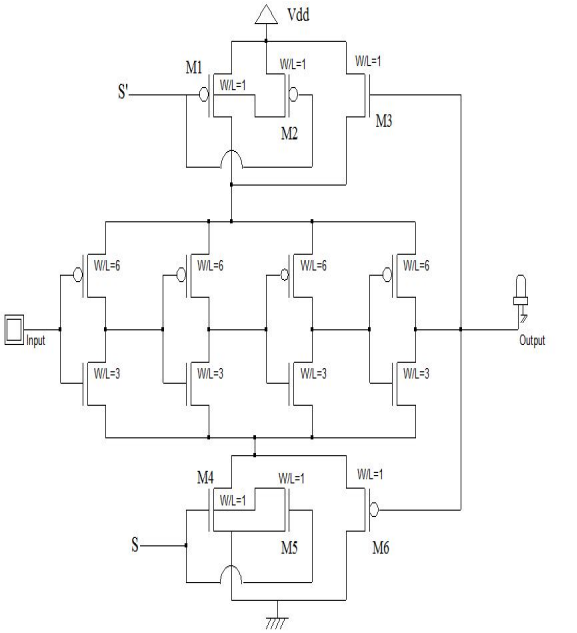


Figure 5: Variable Body Biasing Approach

4. VARIABLE BIASING BIASING PPROACH

To reduce the leakage current in the sleep mode we ensured that the body to source voltage of the sleep transistor is increased. To do that we added a PMOS(M2) and a NMOS (M5) in the previously discussed sleepy keeper circuit (Figure 5). During sleep mode PMOS (M2) is OFF so the body to source voltage of the pull up PMOS (M1) is higher than in the active mode. For a turned off single transistor leakage current (Isub0) can be expressed as follows:

$$I_{sub0} = Ae^{\frac{1}{nV_\theta}(V_{gs0} - V_{th0} - \gamma V_{sb0} + \eta V_{ds0})}(1 - e^{-V_{ds0}/V_\theta})$$

Where, *A C* (*W L*)*V e o ox eff* q = m ; *n* is the sub-threshold swing coefficient, and *Vθ* is the thermal voltage. *Vgs0*, *Vth0*, *Vsb0* and *Vds0* are the gate-to-source voltage, the zero-bias threshold voltage, the base-to-source voltage and the drain-to-source voltage, respectively, γ is the body-bias effect coefficient, and η is the Drain Induced Barrier Lowering (DIBL) coefficient, μ is zero-bias mobility, Cox is the gate-oxide capacitance, W is the width of the transistor, and Leff is the effective channel length. From equation we see that leakage current (Isub0) decreases as Vsb0 increases. As a result of Body effect, Vth also increases which lowers the performance. During the active mode, the performance is improved as the PMOS (M2) is ON which makes the Vth of the pull up PMOS (M1) lower again. The same discussion is applicable for the pull down NMOS (M4) and NMOS (M5). The remaining NMOS (M3) and PMOS (M6) works together for retaining the state in the sleep mode. If the output is high, in the sleep mode, the NMOS (M3) will keep the output high. Similarly, the PMOS (M6) will maintain the state in sleep mode if the output is low.

5. SIMULATION METHODOLOGY

We compare the dual stack approach with Base Case, Sleep, Sleepy Stack and Dual Sleep techniques. Thus, we compare four design approaches in terms of power consumption (dynamic and static), delay and area. To show That the dual stack approach is applicable to general logic and memory design, we choose a chain of 4 inverters (Fig. 4). We use export microwind to estimate delay and power consumption. Area is estimated with the help of MICROWIND.

The inverter chain uses four Inverters each with W/L=6 for PMOS and W/L=3 for NMOS for the base case. Sleep transistors in the sleep approach (Figure 7) are sized such that any sleep transistor between Vdd and a pull-up network takes the size of the largest transistor in the pull-up network, and any sleep transistor between Gnd and a pull-down network takes the size of the largest transistor in the pull-down network. For example, sleep transistors used in the pull-up and pull-down networks of the base case inverter chain have W/L=6 and W/L=3.

Transistors in the stack approach are sized to half of the size of the base case transistors, e.g., transistors used in pull-up and pull-down of the base case inverter chain have W/L=3 and W/L=1.5, respectively. Similarly, transistors, including sleep transistors, in the sleepy stack approach are sized to half of the size of the base case transistors.

6. SIMULATION RESULTS

We measure static power consumption, dynamic power consumption, propagation delay and area for five design

approaches, which are sleep, sleepy stack, dual sleep, dual stack and variable body biasing approach. Figure 8 shows the static power consumption,

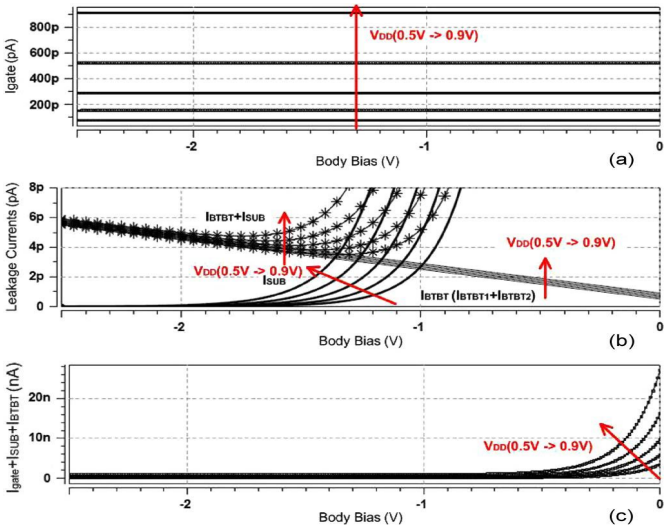


Figure 6 : Standby (*V*GS = 0 V) leakage currents of a 32-nm n-MOSFETwith *t*ox = 0.9 nm and *W/L* = 128 nm/32 nm as a function of body biasvoltage and supply voltage:
a) *I*gate.
(b) I_{SUB}, I_{BTBT}, and $I_{BTBT} + I_{SUB}$.
(c) Total Leakage current = $I_{BTBT} + I_{SUB} + I$gate.

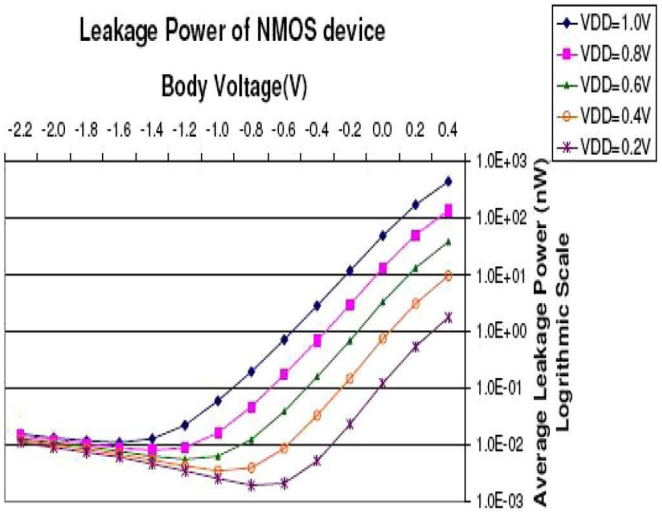


Figure 7: Leakage power of NMOS device under reverse body.

The effect of body bias voltage and supply voltage on the leakage power for an NMOS transistor of 32-nm CMOS technology. At around −0.8 to −2.2 body bias voltage, The leakage power increases due to the highly increased I_{BTBT}, *I*gate has less effect on the power variation. As a result, there is an optimal reverse body bias point that makes the minimal total standby leakage power of a device for each different supply voltage. Therefore, the optimal body bias voltage that reduces the total leakage current is determined by the relationship between I_{SUB} and I_{BTBT}.

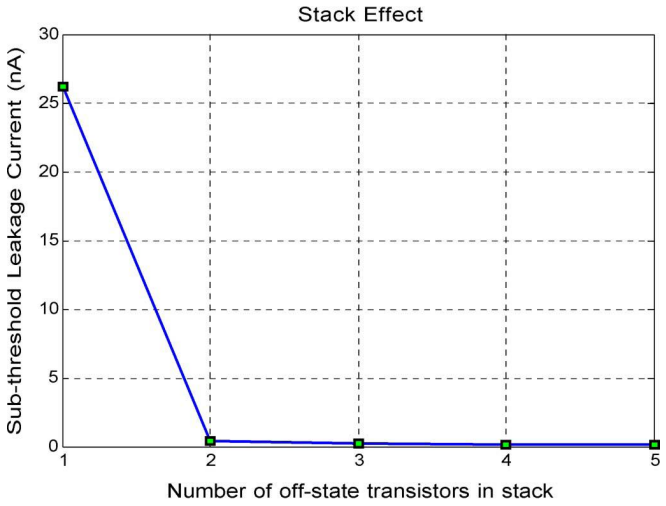
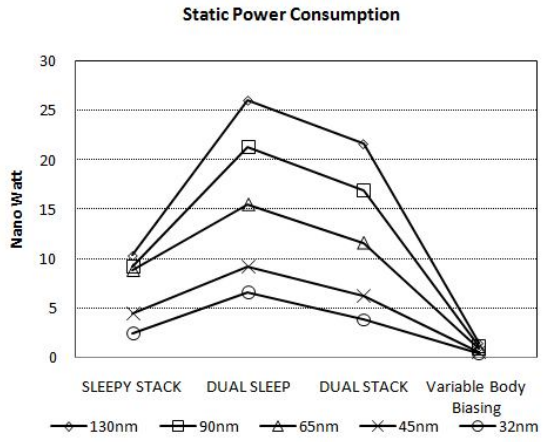


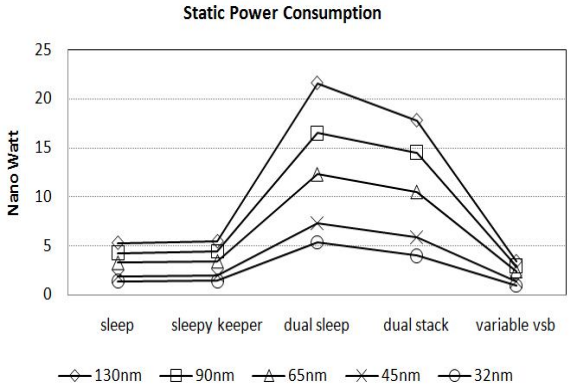
Figure 8 : Leakage current decrease with an increasing number of off transistors in stack (where *V*DD = 0.9 V is applied to 32-nm n-MOSFETs with 0.9-nmoxide thickness and *W/L* = 128 nm/32 nm).

TABLE I
EXPERIMENTAL RESULTS FOR STANDBY LEAKAGE POWER

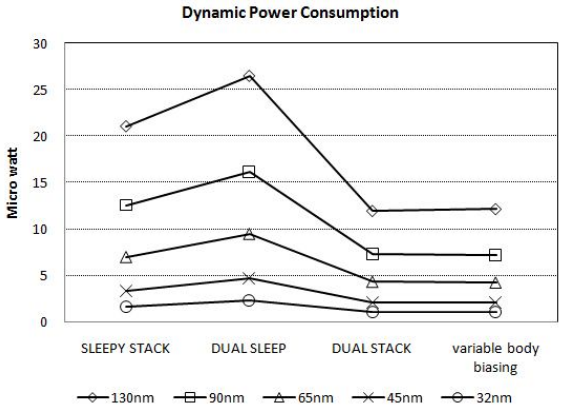
Circuit	# of gates	Function	Leakage(µW):Temperature=25°C		
			Zero Body Bias	*Optimal Body Bias*	*% of Reduction*
C432	160	27-channel interrupt controller	5.880	0.013	452.31%
C499	202	32-bit SEC circuit	14.415	0.030	480.50%
C1908	880	16-bit SEC/DED circuit	14.997	0.040	374.93%
C1355	546	32-bit SEC circuit	21.488	0.039	551.00%
C5315	2307	9-bit ALU	49.687	0.125	397.50%
Circuit	**# of gates**	**Function**	**Leakage(µW):Temperature=100°C**		
			Zero Body Bias	*Optimal Body Bias*	*% of Reduction*
C432	160	27-channel interrupt controller	14.200	0.012	1183.33%
C499	202	32-bit SEC circuit	36.761	0.036	1021.14%
C1908	880	16-bit SEC/DED circuit	35.641	0.043	828.86%
C1355	546	32-bit SEC circuit	53.703	0.036	1491.75%
C5315	2307	9-bit ALU	119.260	0.135	883.41%



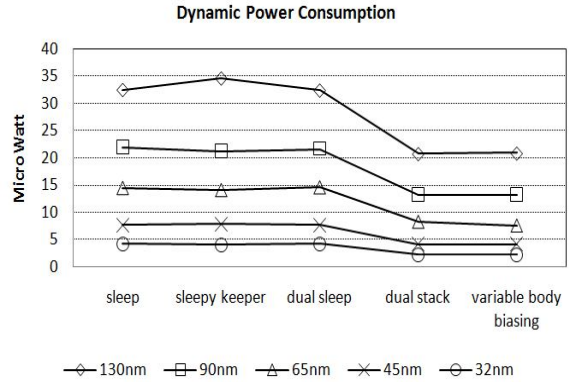
Static Power Comparison (Chain of 4 Inverters)



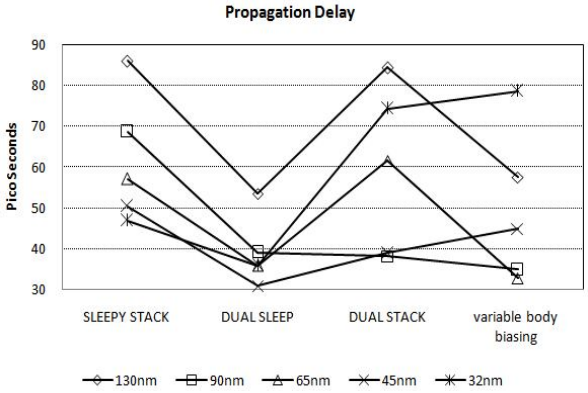
Static Power Comparison (SRAM Cell)



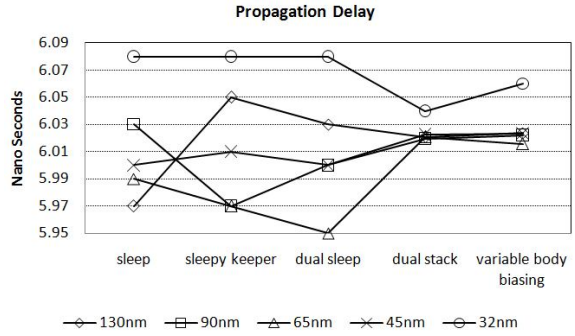
Dynamic Power Comparison (Chain of 4 Inverters)



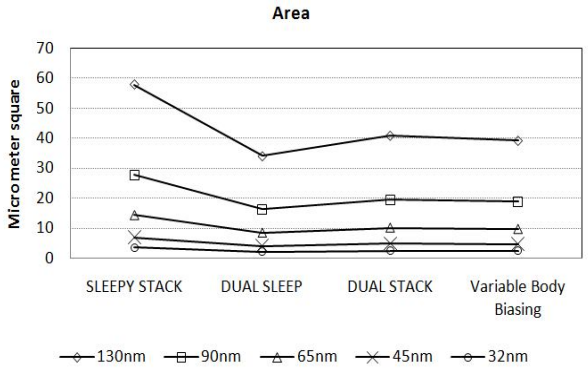
Dynamic Power Comparison (SRAM Cell)



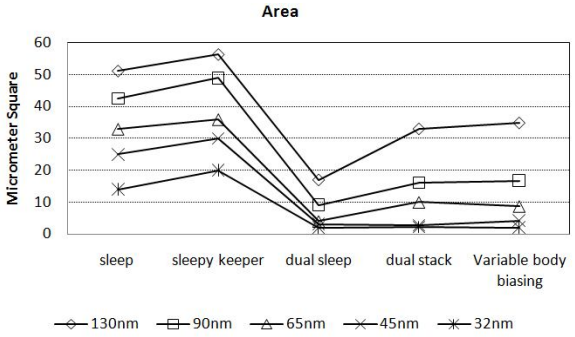
Propagation Delay Comparison (Chain of 4 Inverters)



Propagation Delay Comparison (SRAM Cell)



Area Comparison (Chain of 4 Inverters)



Area Comparison (SRAM Cell)

The comparisons of Variable body biasing approach using65 nm technology with the existing methods for a chain of fourinverters and for a SRAM cell are summarized in Table II andTable III, respectively. Here '+' denotes improved and '-'denotes degraded performance.

TABLE II
COMPARISON OF V_{BB} APPROACH FOR A CHAIN OF FOUR INVERTERS

Methods	delay	Static Power	Dynamic Power	Area
Dual sleep	+8.37%	+94.7%	+55.4%	-15.16%
Dual stack	+46.67%	+92.93%	+2.09%	+4.09%

TABLE III
COMPARISON OF V_{BB} APPROACH FOR A SRAM CELL

Methods	delay	Static Power	Dynamic Power	Area
Dual sleep	-1.1%	+80.49%	+47.89%	-74.28%
Dual stack	+0.08%	+77.14%	+8.26%	+12.86%

Power delay products for a chain of four inverters are 0.34fJ, 0.266fJ and 0.139fJ for dual sleep, dual stack and Variable Body Biasing, respectively. Therefore, the Variable Body Biasing approach shows the least power delay product among all.

7. CONCLUSION

The new circuit design technique for minimizing the leakage power must be developed along with the device scaling. To reduce the standby leakage power, this paper has presented novel design technique that generates the optimal Body scaling during standby mode. By monitoring the BTBT leakage current (*I*BTBT) and the sub threshold leakage current(*I*SUB), the optimal body-bias voltage is automatically generated and continuously adjusted by the control loop. By tuning the body bias voltage using the leakage-monitoring circuit, the circuit can be biased at the optimal point where the sub threshold leakage current and the BTBT leakage current are balanced to accomplish the minimum leakage power. Miniaturization of CMOS technology achieving high performance has resulted in increase of leakage power dissipation. We have presented an efficient methodology for reducing leakage power in VLSI design. Our Variable Body Biasing approach shows improved results in terms of static power, dynamic power and power delay product. It gives theCMOS circuit designers another option in designing integrated circuits more efficiently.

REFERENCES

1. S. Mutoh et al. **1-V Power Supply High-speed Digital Circuit Technology with Multithreshold-Voltage CMOS**, IEEE Journal of Solis-State Circuits, Vol. 30, No. 8, pp. 847-854, August 1995.

2. M. Powell, S.-H. Yang, B. Falsafi, K. Roy and T. N. Vijaykumar. **Gated-Vdd: A Circuit Technique to Reduce Leakage in Deepsubmicron Cache Memories**, International Symposium on Low Power Electronics and Design, pp. 90-95, July 2000.

3. J.C. Park, V. J. Mooney III and P. Pfeiffenberger. **Sleepy Stack Reduction of Leakage Power," Proceeding of the International Workshop on Power and Timing Modeling,** Optimization and Simulation, pp. 148-158, September 2004.

4. J. Park. **Sleepy Stack: a New Approach to Low Power VLSI and Memory**, Ph.D. Dissertation, School of Electrical and Computer Engineering, Georgia Institute of Technology, 2005. [Online]. Available http://etd.gatech.edu/theses

5. M. Powell, S.-H. Yang, B. Falsafi, K. Roy and T. N. Vijaykumar. **Gated-Vdd: A Circuit Technique to Reduce Leakage in Deep submicron Cache Memories**, Proc. of International Symposium on Low Power Electronics and Design, pp. 90-95, July 2000.

6. J.C. Park, V. J. Mooney III and P. Pfeiffenberger. **Sleepy Stack Reduction of Leakage Power," Proc. of the International Workshop on Power and Timing Modeling**, Optimization and Simulation, pp. 148- 158, September 2004.