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Efficient Weighted Pattern Generation Technique With Low Hardware Overhead

K.Veena Madhavi[1], Mrs. M.Nirmala[2]

[1] M.Tech Student, LIET, Hyderabad, A.P., India, Email: veenamadhavi999@gmail.com

[2]Associate Professor, ECE, LIET, Hyderabad, A.P., India, Email: nirmalaecelords@gmail.com

ABSTRACT

Weighted pseudorandom built-in self test (BIST) schemes have been utilized in order to drive down the number of vectors to achieve complete fault coverage in BIST applications. Weighted sets comprising three weights, namely 0, 1, and 0.5 have been successfully utilized so far for test pattern generation, since they result in both low testing time and low consumed power. In this paper an accumulator-based 3-weight test pattern generation scheme is presented; the proposed scheme generates set of patterns with weights 0, 0.5, and 1. Since accumulators are commonly found in current VLSI chips, this scheme can be efficiently utilized to drive down the hardware of BIST pattern generation, as well. Comparisons with previously presented schemes indicate that the proposed scheme compares favorably with respect to the required hardware.

Index Terms : BIST, test per clock, VLSI testing, weighted test pattern generation

1. INTRODUCTION

Built in self test (BIST) generators such as pseudorandom Built in self test generators are extensively used to test the integrated circuits and systems. A large number of pseudorandom generators include linear feedback shift registers (LFSR'S) [1], cellular automata [2], accumulators driven by a constant value [3].some faults are hard to detect in a circuit so a large number of random patters are to be generated before high fault coverage is achieved. A weighted pseudorandom techniques have been proposed, where inputs are biased by changing the probability of "O" or "1" on a given input from 0.5 for pure pseudorandom tests to some other value[10][13].Usually weighted random pattern generation technique that rely on a single weight assignment fail to achieve complete fault coverage using number of test patterns even though the weights are suitable for most of the faults. To detect faults with these weight assignments some faults require long test sequences to be detected if they do not match their and propagation requirements. Different faults require different weight input combinations applied to the circuit so that a small number of patterns can detect all faults for this a multiple weight assignments are suggested [4]. Approaches to derive weight assignments for a given deterministic tests are efficient as they allow complete fault coverage with small number a test patterns [10].

Hardware Implementation cost is minimized by multiple weight assignments by using the weights as 0, 1, and 0.5. The outputs remain constant as either 0 or 1 and other value changes as 0.5 i.e., pseudorandom. Therefore this reduces the hardware overhead and the power consumption as some of the devices under test (DUT) inputs remain steady as 0 or 1 during specific test session [20].

Pomeranz and Reddy [5] proposed a 3 weight pattern generation scheme relying on the weights 0, 1 and 0.5. The choice of the weights 0, 1 and 0.5 was done in order to minimize the hardware implementation cost. Wang [8] [12] proposed a 3 weight random pattern generator based on scan chains using the weights 0, 1 and 0.5[5]. Zhang [9] renovated the interest in the 3 weight pattern generation schemes, proposing an efficient compaction scheme for the 3 weight patterns 0, 1, and 0.5 has practical interest since it combines low implementation cost with low test time. Current VLSI circuits such as data path architecture or digital signal processing chips commonly contain arithmetic modules such as accumulators or arithmetic logic units.

The basic of ABIST (arithmetic BIST) [6] is to utilize accumulators for built in testing by the compression

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of DUT responses and has resulted in low hardware overhead and low impact on the circuit normal operating speed [14]-[19].In [7] if the input patters are properly selected then the test vectors generated by the accumulator whose inputs are driven by a constant pattern can be pseudo random characteristics. Modules containing hard o detect faults may require extra test hardware either by inserting test points in the logic or by storing extra deterministic test patterns[16][17].

The accumulator based weighted pattern generation scheme proposed [11] generates test patterns having the three weights 0, 1 and 0.5; this is used to reduce the test application time. The scheme proposed in [11] possesses three major drawbacks: 1) it can be utilized only in the case that the adder of the accumulator is a ripple carry adder, 2) It requires redesigning the accumulator, requires redesign of the core of the data path, it is not used in current BIST scheme, 3) it increases delay as it effects the normal operating speed of the adder.

In this paper novel scheme for accumulator based 3-weight pattern generation is presented and it copes with the inherent drawbacks of the scheme proposed in [11].More precisely: 1) it does not impose any requirements about the redesign of the adder, 2) it does not require any modification of the adder, 3) it does not affect the operating speed of the adder.

This paper is organized as follows. In section 2, the idea of the accumulator based 3-weight generation is presented. In section 3, design methodology to generate the 3-weight patterns utilizing the accumulator is presented. In section 4, the design process of the 3- weight pattern generation by using the accumulator is presented.

2. ACCUMULATOR BASED 3-WEIGHT PATTERN GENERATION

Let us illustrate the idea of an accumulator based 3-weight pattern generation by means of an example. Let us consider the test set for the C17 benchmark [21][12] given in table 1.From the deterministic test set in order to apply the 3- weight pattern generation schemes, one of the schemes proposed in [5], [8] and [9] can be utilized.

Accordingly ,a typical weight assignment procedure involves separating the test set into two subsets S1 and S2 as follows: S1={T1,T4} and S2={T2,T3}.the weight assignment for these subsets is W(S1)={-,-,1,-,1} and W(S2)={-,-,0,1,0},where "–"denotes a weight assignment of 0.5.

A "1" indicates that the input is constantly driven by logic 1 value and a "0" indicates that the input is constantly driven by logic 0 value. In the subsets S1,inputs A[2] and A[0] are constantly driven by logic "1" while the inputs A[4],A[3] and A[1] are pseudo randomly generated value of weight "0.5". for the subsets S2,inputs A[2] and A[0] are constantly driven by logic "0" while the inputs A[1] is driven by "1"and inputs A[4] and A[3] are pseudo randomly generated value of weight "0.5".

Table 1: Test Set For C17 Benchmark

Test vector	Inputs A[4:0]
T1	00101
T2	01010
T3	10010
T4	11111

Table 2: Truth Table Of Full Adder

#	Cin	A[i]	B[i]	S[i]	C_{out}	Comment
1	0	0	0	0	0	
2	**0**	0	1	1	**0**	$C_{out}=C_{in}$
3	**0**	1	0	1	**0**	$C_{out}=C_{in}$
4	0	1	1	0	1	
5	1	0	0	1	0	
6	**1**	0	1	0	**1**	$C_{out}=C_{in}$
7	**1**	1	0	0	**1**	$C_{out}=C_{in}$
8	1	1	1	1	1	

The above reasons, configures the accumulator where the following conditions are met: 1)an accumulator output can be constantly driven by logic "1" or logic "0" and, 2)an accumulator cell with its output constantly driven to "1" or "0" allows the carry input to carry to its carry output unchanged. This condition requires to effectively generate the pseudorandom patterns in the accumulator outputs whose weight assignment is "-".

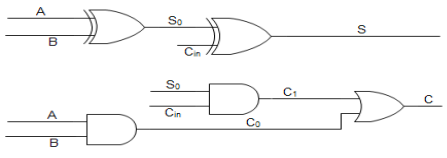

Figure 1: Full Adder Circuit

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In the full adder circuit let us generate the faults and generate the patterns through them .there are 8 nets so 16 faults can be generated from the full adder circuit. The faults for each net are stuck-at-0 fault and stuck-at-1 fault. While generating these faults controllability and observability of these faults must be observed.

3. DESIGN METHODOLOGY

The implementation of the weighted pattern generation scheme is based on the full adder truth table presented in table 2.From the table 2 we observe that the lines #2,#3,#6 and #7,$C_{out} = C_{in}$, in order to transfer the carry input to the carry output it is sufficient to set A[i]=NOT(B[i]).

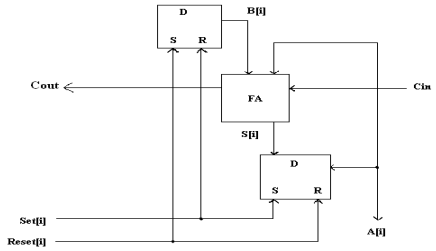

Figure 2: Accumulator Cell

The implementation of the proposed weighted pattern generation scheme is based on the accumulator cell presented in fig 2 that consists of a full adder(FA) cell and D-type flip flop with asynchronous set and reset inputs whose output is also driven to one of the full adder inputs. A LPSR is used in the 3-weight pattern without loss of generality, that the set and reset are active high signals. The respective cell of the driving register B[i] is also seen. One out of three configurations can be utilized as shown in Fig 3.

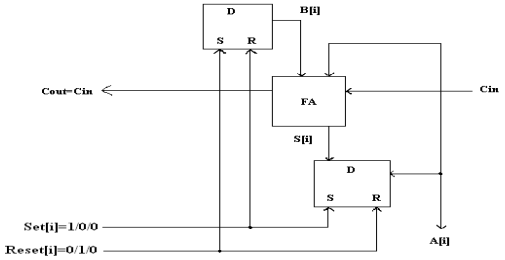

Figure 3: Configurations of The Accumulator Cell

In the Fig 3(a), the configuration that drives the DUT inputs when A[i] =1 is required. Set[i] =1 and reset[i] =0and hence A[i] =1 and B[i] =0.Then the output is equal to 1 and C_{in} is transfers to C_{out}. In fig 3(b), the configuration that drives the DUT inputs when A[i] =0 is required. Set[i]=0 and reset[i]=1and hence A[I]=0 AND b[i]=1.Then the output is equal to 0 and C_{in} is transferred to C_{out}.

In fig 3(c), the configuration that drives the DUT inputs when A[i] = "-" is required. Set[i]=0 and reset[i]=0.The D input of FF of register B is driven by either 1 or 0,depending on the value that will be added to the accumulator inputs in order to generate random patterns to the inputs of the DUT.

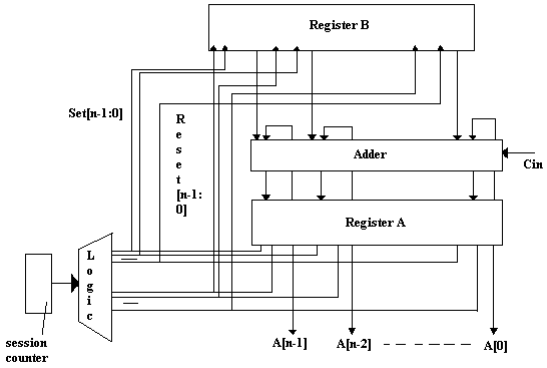

Figure 4: Proposed Scheme

In fig 4 the general configuration of the proposed scheme is presented. The logic nodule provides that set [n-1:0] and reset [n-1:0] signals that drive the S and R inputs of the register A and register B inputs.

The signals that drive the S-inputs of the flip flop LFF of register A also drive the inputs of the F of register B and vice versa.

4. DESIGN PROCESS

Let us consider a circuit with different gates having 10 inputs and 3 outputs. As there are 22 nets therefore 42 faults can be generated from these nets. The faults are struck at 0 faults and struck at 1 fault.

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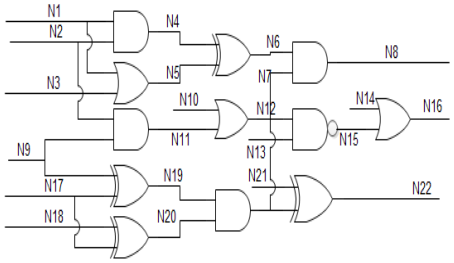

Figure 5: 10-Input Circuit Design

From this fault patterns are generated. The controllability and observability of the faults should be observed. At each pattern different number of faults is covered.

Table 3: Generated Patterns

	P1	P2	P3	P4	P5	P6
N1	1	1	0	0	X	X
N2	1	0	1	0	X	X
N3	X	X	1	0	X	X
N9	0	0	1	1	0	1
N10	0	1	0	1	1	X
N13	1	1	1	0	1	X
N14	0	0	0	0	1	X
N17	1	1	0	0	1	1
N18	0	0	1	1	1	0
N21	X	X	X	X	0	0

A Typical weight assignment procedure involves separating the patterns into 3 subsets:S1,S2 and S3 as follows:S1={P1,P2},S2={P3,P4},S3={P4,P5}.
The weight assignments for these subsets are W(S1)={1,-,1,0,-,1,0,1,0,0},W(S2)={0,1,1,-,-1-,-,1,0},W(S3)={0,0,0,1,1,0,0,-,-,0}.where "_" denotes the pseudorandom value,"1" denotes input is constantly driven by logic 1,"0" denotes input is constantly driven by logic 0.

Table 4: Subset Patterns With Weights

	(P1,P2)	(P3,P5)	(P4,P6)
N1	1	0	0
N2	0.5	1	0
N3	1	1	0
N9	0	0.5	1
N10	0.5	0.5	1
N13	1	1	0
N14	0	0.5	0
N17	1	0.5	0.5
N18	0	1	0.5
N21	0	0	0

At different ns of time different patterns are generated. By using accumulator based3 weight pattern generation using LFSR all the patterns are efficiently generated.

Table 5: Test Time In Ns

PATTERN	TIME IN ns
11X001010X	2100
10X011010X	1100
011101001X	7100
000110001X	3900
XXX0111110	2500
XXX1XXX100	4900

RESULT:

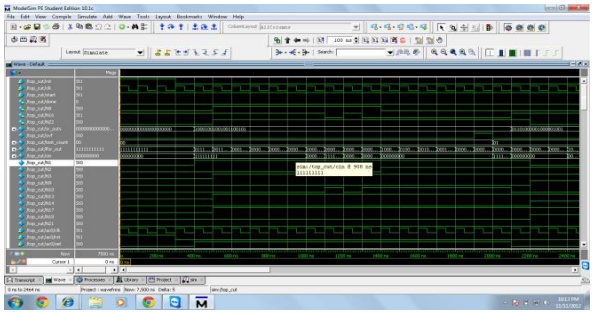

Figure 6: 3-Weight BIST

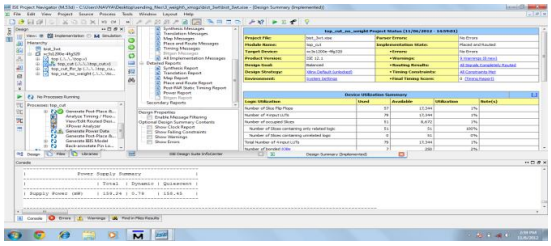

Figure 7: Low hardware and dynamic power

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5. CONCLUSION

We have presented an accumulator-based 3-weight (0, 0.5, and 1) test-per-clock generation scheme, which can be utilized to efficiently generate weighted patterns without altering the structure of the adder. Accumulator-based 3-weight pattern generation technique [11] indicate that the hardware overhead of the proposed scheme is lower, while at the same time no redesign of the accumulator is imposed, thus resulting in reduction in test application time. Comparision with the previous papers which uses no-weight and weighted pattern generation technique, this weighted pattern generation with accumulator covers all the patterns and the test time is also less. There is 100% fault coverage without reuse of the external hardware and therefore it is low hardware overhead.

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