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SIMULATION OF A SPACE VECTOR PWM CONTROLLER FOR A THREE-LEVEL VOLTAGE-FED INVERTER MOTOR DRIVE

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***Abstract*--Multilevel voltage-fed inverters with space vector pulse width modulation(SVPWM) strategy are gained importance in high power high performance industrial drive applications. This paper proposes a new simplified space vector PWM method for a three-level inverter fed induction motor drive. The three level inverter has large number of switching states as compared to a two level inverter. In the proposed scheme, three-level space vector PWM is easily implemented as conventional two-level space vector PWM inverter. Therefore, the proposed method can also be applied to multilevel inverters. In this work, a three-level inverter using space vector modulation strategy has been modeled and simulated. Simulation results are presented for various operation conditions using R-L load and motor load to verify the system model.**

Index terms **- multi-phase drives, space vector pulse width modulation(SVPWM), voltage source inverters(VSIs)**

1. INTRODUCTION

The developments in power electronics and semiconductor technology have lead improvements in power electronic systems. Hence, different circuit configurations namely multilevel inverters have became popular and considerable interest by researcher are given on them. Three-level voltage-fed PWM inverters are recently showing popularity for multi-megawatt industrial drive applications. The main reason for this popularity is that the output voltage waveforms in multilevel inverters can be generated at low switching frequencies with high efficiency and low distortion and large voltage between the series devices is easily shared. Space vector PWM (SVPWM) technique is one of the most popular techniques gained interest recently. This technique results in higher magnitude of fundamental output voltage available as compared to sinusoidal PWM. However, SVPWM algorithm used in three-level inverters is more complex because of large number of inverter switching states. One of the advantages of multilevel inverters is that the voltage stress on each switching device is reduced. In addition, multilevel waveforms feature have less harmonic content compared to two level waveforms operating at the same switching frequency. In this paper, modelling and simulation of a multilevel inverter using cascaded inverters with separated DC sources have been performed with R-L and motor load using Simulink MATLAB package program. In multilevel inverters, it is easy to reach high voltage levels in high power applications with lower harmonic distortion and switching frequency, which is very difficult to get this performance with conventional two level inverters.

1.1 Theory

The Space Vector PWM generation module accepts modulation index commands and generates the appropriate gate drive waveforms for each PWM cycle. This section describes the operation and configuration of the SVPWM module.

A three-phase 2-level inverter with dc link configuration can have eight possible switching states, which generates output voltage of the inverter. Each inverter switching state generates a voltage Space Vector (V1 to V6 active vectors, V7 and V8 zero voltage vectors) in the Space Vector plane (Figure :space vector diagram). The magnitude of each active vector(V1to V6) is 2/3 Vdc (dc bus voltage).

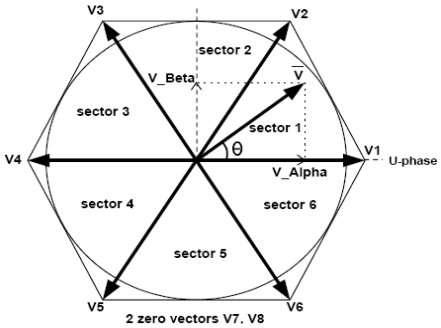

Fig1. Space Vector Diagram

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1.2 Transfer Characteristics

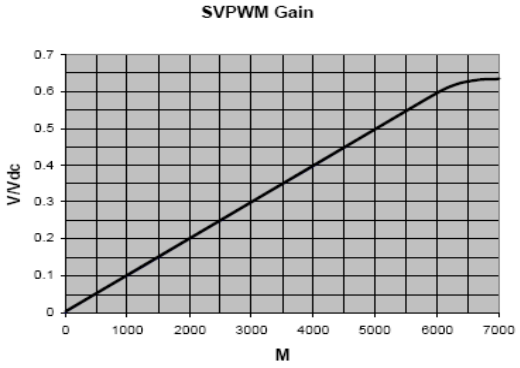

Fig2.Transfer characteristics

2.PWM Operation

Upon receiving the modulation index commands (UAlpha and UBeta) the sub-module SVPWM_Tm starts its calculations at the rising edge of the PWM Load signal. The SVPWM_Tm module implements an algorithm that selects (based on sector determination) the active space vectors (V1 to V6) being used and calculates the appropriate time duration (w.r.t. one PWM cycle) for each active vector. The appropriated zero vectors are also being selected. The SVPWM_Tm module consumes 11 clock cycles typically and 35 clock cycles (worst case Tr) in over modulation cases. At the falling edge of nSYNC, a new set of Space Vector times and vectors are readily available for actual PWM generation (PhaseU, PhaseV, PhaseW) by sub module PwmGeneration. It is crucial to trigger PwmLoad at least 35 clock cycles prior to the falling edge of nSYNC signal; otherwise new modulation commands will not be implemented at the earliest PWM cycle.

The above Figures voltage vector rescaling illustrates the PWM waveforms for a voltage vector locates in sector I of the Space Vector plane (shown in Figure). The gating pattern outputs (PWMUH … PWMWL) include dead time insertion

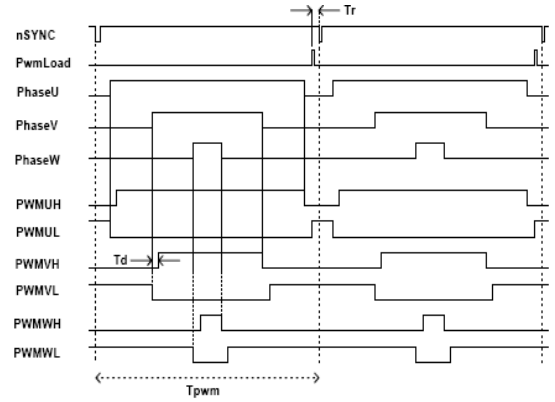

Fig3.PWM Operation

2.1 3-phase Space Vector PWM

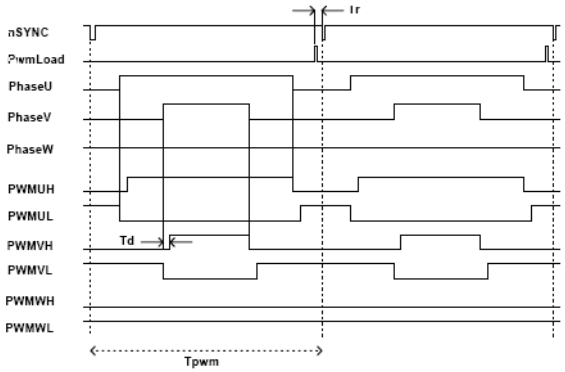

Fig 4.3-phase Space vector PWM

2.3 Symmetrical Mode Operation

There are two modes of operation available for PWM waveform generation, namely the Center Aligned Symmetrical PWM (Figure) and the Center Aligned Asymmetrical PWM (Figure)The volt-sec can be changed every half a PWM cycle (Tpwm) since PwmLoad occurs every half a PWM cycle (compare Figure :symmetrical pwm and Figure :asymmetrical PWM). With Symmetrical PWM mode, the inverter voltage Config = 0), the inverter voltage can be changed at two times the rate of the switching frequency. This will provide an increase in voltage control bandwidth, however, at the expense of increased current harmonic

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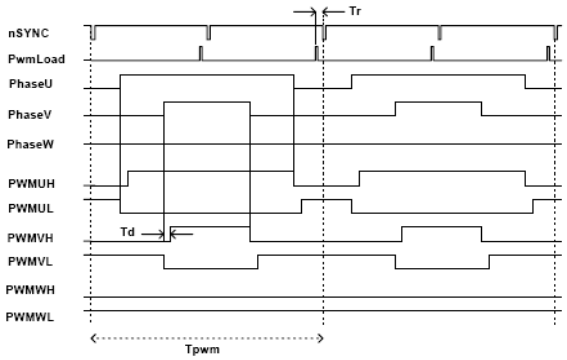

Fig 5. Symmetrical Mode Operation

Asymmetrical PWM Mode

Three-Phase and Two-Phase Modulation

Three-phase and two-phase Space Vector PWM modulation options are provided for the IRMCx203. The Volt-sec generated by the two PWM strategies are identical; however with 2-phase modulation the switching losses can be reduced significantly, especially when high switching frequency (>10Khz) is employed. Figure: three-phase and two phase modulation shows the switching pattern for one PWM cycle when the voltage vector is inside sector 1

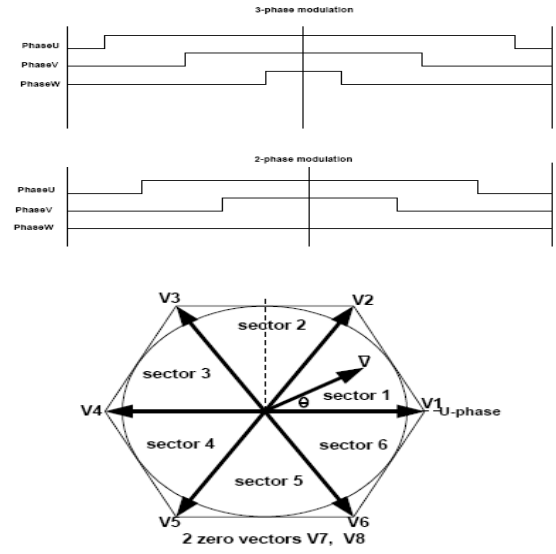

Fig6.Three Phase and Two Phase Modulation

The field Two Phase PWM of the PWM Config write register group provides selection of three-phase or two-phase modulation. The default setting is three-phase modulation. Successful operation of two-phase modulation in the entire speed operating range will depend on hardware configuration. If the gate driver employs a bootstrap power supply strategy, misoperation will occur at low motor fundamental frequencies (< 2Hz) under two-phase modulation control.

2.4 Sinusoidal Pulse Width Modulation

In many industrial applications, Sinusoidal Pulse Width Modulation (SPWM), also called Sine coded Pulse Width Modulation, is used to control the inverter output voltage. SPWM maintains good performance of the drive in the entire range of operation between zero and 78 percent of the value that swould be reached by square-wave operation. If the modulation index exceeds this value, linear relationship between modulation index and output voltage is not maintained and the over-modulation methods are required

2.5 Space Vector Pulse Width Modulation

A different approach to SPWM is based on the space vector representation of voltages in the d, q plane. The d, q components are found by Park transform, where the total power, as well as the impedance, remains unchanged.

Fig: space vector shows 8 space vectors in according to 8 switching positions of inverter, V* is the phase-to-center voltage which is obtained by proper selection of adjacent vectors V1 and V2.

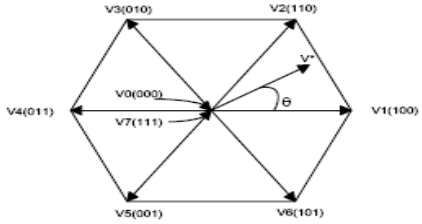

Fig7.Inverter output voltage space vector

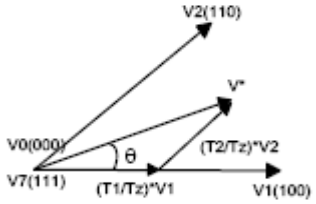

Fig8.Determination of Switching times

The reference space vector V* is given by Equation (1), where T1, T2 are the intervals of application of vector V1 and V2 respectively, and zero vectors V0 and V7 are selected for T0.

$$V^* Tz = V1 *T1 + V2 *T2 + V0 *(T0/2) + V7 *(T0/2) \quad \ldots\ldots(1)$$

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Space Vector Pulse Width Modulation (continued)

Fig. below shows that the inverter switching state for the period T1 for vector V1 and for vector V2, resulting switching patterns of each phase of inverter are shown in Fig. pulse pattern of space vector PWM.

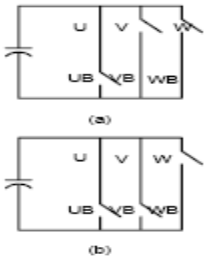


Fig9.Inverter switching state for (a)V1, (b) V2

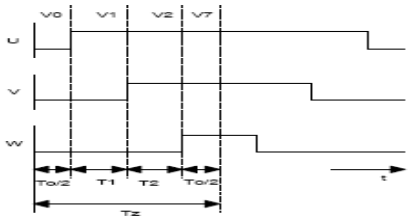


Fig10.Pulse pattern of Space vector PWM

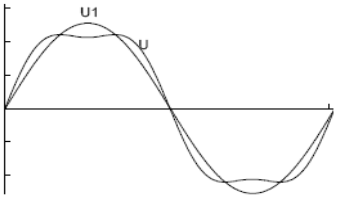


Fig11. Comparison

In Fig11- comparison, U is the phase to- center voltage containing the triple order harmonics that are generated by space vector PWM, and U1 is the sinusoidal reference voltage. But the triple order harmonics are not appeared in the phase-to-phase voltage as well. This leads to the higher modulation index compared to the SPWM.

3. Comparison of SPWM and Space Vector PWM

As mentioned above, SPWM only reaches to 78 percent of square wave operation, but the amplitude of maximum possible voltage is 90 percent of square-wave in the case of space vector PWM.

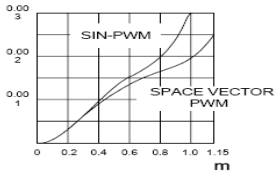
The maximum phase-to-center voltage by sinusoidal and space vector PWM are respectively

Vmax = Vdc/2 : Sinusoidal PWM

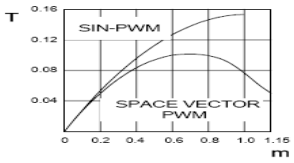
Vmax = Vdc/√3 : Space Vector PWM

Where, Vdc is DC-Link voltage.

This means that Space Vector PWM can produce about 15 percent higher than Sinusoidal PWM in output voltage.



(a)rms harmonic current



(b) torque harmonics

Fig12.(a)rms harmonic current (b) torque harmonics

3.1 SVM PWM Technique

The Pulse Width modulation technique permits to obtain three phase system voltages, which can be applied to the controlled output. Space Vector Modulation (SVM) principle differs from other PWM processes in the fact that all three drive signals for the inverter will be created simultaneously. The implementation of SVM process in digital systems necessitates less operation time and also less program memory.

The SVM algorithm is based on the principle of the space vector u*, which describes all three output voltages ua, ub and uc :

u* = 2/3 . (ua + a . ub + a2 . uc) ……(2)

where a = -1/2 + j . v3/2

We can distinguish six sectors limited by eight discrete vectors u0…u7

(fig:- inverter output voltage space vector), which correspond to the 23 = 8 possible switching states of the power switches of the inverter.

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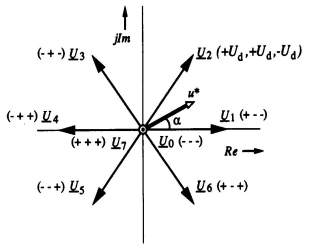


Fig13.space vectors

3.2 Space vector Modulation

The amplitude of u0 and u7 equals 0. The other vectors u1…u6 have the same amplitude and are 60 degrees shifted.

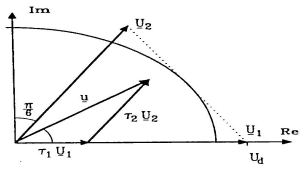
By varying the relative on-switching time Tc of the different vectors, the space vector u* and also the output voltages ua, ub and uc can be varied and is defined as:

$$ua = Re (u^*)$$

$$ub = Re (u^* . a^{-1})$$

$$uc = Re (u^* . a^{-2}) \quad \text{……(3)}$$

During a switching period Tc and considering for example the first sector, the vectors u0, u1 and u2 will be switched on alternatively.



Definition of the Space vector

Depending on the switching times t0, t1 and t2 the space vector u* is defined as:

$$u^* = 1/Tc . (t0 . u0 + t1 . u1 + t2 . u2)$$

$$u^* = t0 . u0 + t1 . u1 + t2 .$$

$$u^* = t1 . u1 + t2 . u2 \quad \text{…….. (4)}$$

where

$$t0 + t1 + t2 = Tc \text{ and}$$

$$t0 + t1 + t2 = 1$$

t0, t1 and t2 are the relative values of the on switching times.

They are defined as:

$$t1 = m . \cos (a + p/6)$$

$$t2 = m . \sin a$$

$$t0 = 1 - t1 - t2$$

Their values are implemented in a table for a modulation factor m = 1. Then it will be easy to calculate the space vector u* and the output voltages ua, ub and uc. The voltage vector u* can be provided directly by the optimal vector control laws w1, v_{sa} and v_{sb}. In order to generate the phase voltages ua, ub and uc corresponding to the desired voltage vector u* the following SVM strategy is proposed.

4. Three-Dimensional Vector Representation

A multilevel converter can synthesize output voltages from many discrete voltage levels. Therefore, the functional diagram of an n-level diode-clamped converter can be represented as shown in Fig below.

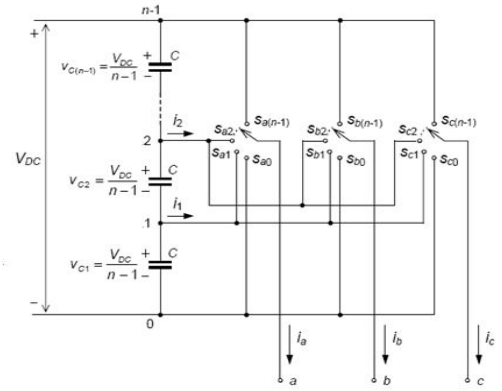


Fig14: functional diagram of n-level diode clamped converter

Each switching state, or combination of phase-leg switches, produces a defined set of three-phase voltages, which can be represented as vectors in the three- dimensional Euclidean diagram (Fig. three dimensional space vector diagram)

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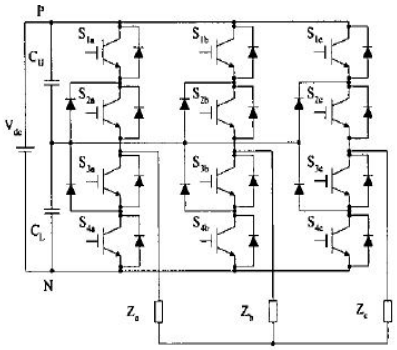

Fig15.Circuit diagram of a three- level diode- clamped inverter

In this project, a simple method is proposed to implement the processes above and the procedure introduced is common for both the low-level and high-level inverters. The proposed algorithm for a three-level inverter (shown **as** Fig.circuit diagram of a three –level diode –clamped inverter) is verified by simulation and experiment.

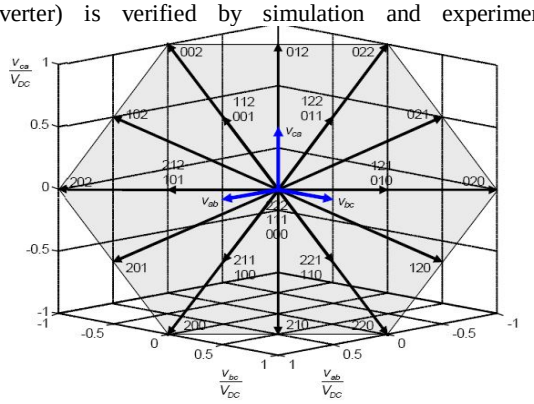

Fig16. Three dimensional SV diagram

The variables represented in Fig:three dimensional SV diagram are the line-to-line voltages from a three- level converter, as follows:

$$\vec{\mathbf{v}} = [v_{ab} \quad v_{bc} \quad v_{ca}]^{\mathsf{T}}, \quad \text{or} \quad \vec{\mathbf{v}} = \frac{V_{DC}}{n-1}[i-j \quad j-k \quad k-i]^{\mathsf{T}}, \quad \text{...(5)}$$

where *i, j, k* ∈ [0, … , *n*-1], which define the position of the single-pole n-throw switches of phases *a*, *b* and *c*, respectively. The vectors are labeled as (*i, j, k*) in order to simplify their notation.

Because of Kirchhoff's Law, the sum of the line-to-line voltages is always zero; this is really an equation of the plane in the line-to-line coordinate system. This means that all of the vectors of a multilevel converter lie in a plane, and that is how they are usually represented. When the phase voltages are represented in the three-dimensional diagram, they do not lie in a plane. However, they can be projected into a plane, thereby representing an equivalent two-dimensional diagram.Coming back to the three-dimensional representation, a voltage reference vector r (*m*) that must be synthesized by PWM-averaged approximation can also be represented in vector form, as follows

$$\vec{m} = \hat{V}_{LL}\begin{bmatrix} \cos(\omega t + \theta_o) \\ \cos(\omega t - \frac{2\pi}{3} + \theta_o) \\ \cos(\omega t + \frac{2\pi}{3} + \theta_o) \end{bmatrix}, \quad \text{..... (6)}$$

where $V_{LL,}$ is the amplitude of the line-to-line voltages. Since this vector has only two degrees of freedom, it also lies on the same plane as the switching vectors. Using the definition of vector norm, the length of the reference vector is

$$|\vec{m}| = \sqrt{|\vec{m}|^2 + |\vec{m}|^2} = \sqrt{\frac{3}{2}}\hat{V}_{LL}, \quad \text{.(7)}$$

while by the same definition, the length of the longest switching vector is

$$\left|\vec{V}_{\max}\right| = \sqrt{2}\, V_{DC}. \quad \text{..... (8)}$$

The maximum length of the reference vector (10) that can be synthesized in steady-state conditions equals the radius of the largest circle that can be inscribed in the outer hexagon. Therefore, the maximum length of the reference vector is

$$|\vec{m}_{\max}| = \frac{\sqrt{3}}{2}\left|\vec{V}_{\max}\right|. \quad \text{..... (9)}$$

By substituting (11) into (12) and comparing the resulting equation with (10), the maximum amplitude of the undistorted line-to-line voltage that can be synthesized is

$$\hat{V}_{LL\max} = V_{DC}. \quad \text{..... (10)}$$

4.1 Two-Dimensional Vector Representation

The Clarke's Transformation allows the three-dimensional vector representation to be displayed in a two-dimensional diagram. Given three output voltages of the converter (v_{0a} v_{b0} and v_{0c}) , the projection in a plane αβ (v_{α}, v_{β}) of a three-dimensional vector is

$$\vec{V} = v_{\alpha} + j v_{\beta} = v_{a0}\vec{a}^0 + v_{b0}\vec{a}^1 + v_{c0}\vec{a}^2, \quad \text{... (11)}$$

Where $\vec{a} = e^{j\frac{2\pi}{3}}$.

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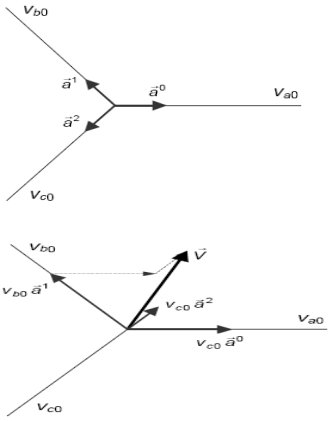
Fig. below shows the three unitary director vectors of this transformation, while Fig shows an example for the case in which *Vao*_= 200 *V*, *Vbo*=300 *V*, and *Vco*= -100 *V*

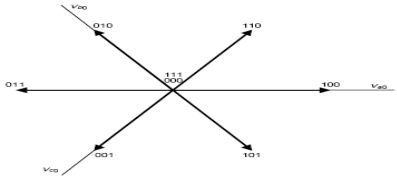


Clark's Transformation: fig17(a) director vectors,and (b) example of spatial vector for $v_{0a=}$ 200 V, v_{b0}=300 V, and v c0=-100 V

The aim of the SVM is to generate a reference vector (*m*) in the same plane for each modulation cycle. As the reference vector may not be the same as any vector produced by the converter, its average value can be generated using more than one vector per modulation cycle by PWM-averaged approximation. Selecting proper vectors and applying them in a suitable order helps the devices achieve low switching frequencies.

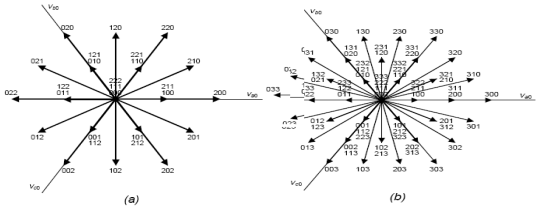
In steady-state conditions, the reference vector rotates at a constant angular speed (ω), which defines the frequency of the output voltages. The amplitude of the fundamentals of those voltages is proportional to the length of the reference vector.

There are eight possible states for the two-level converter (*n* =2 =8), which produce the voltage vectors shown in Fig. 3.4. Six of these vectors have equal lengths and are located every sixty degrees (100, 110, 010, 011, 001, 101). The other two vectors are in the origin because of their null lengths (000, 111)



4.2 SV diagram of the two-level converter

The SV diagrams of the three-level and four-level converters have twenty-seven and sixty-four vectors, respectively



SV diagrams of18. (a) the three-level converter, and (b) the four-level converter

The redundant vectors in the diagram produce the same line-to-line voltages. The three-level converter has six double vectors and one triple vector in the origin. The four-level inverter has twelve double vectors, six triple vectors and one tetra vector in the origin. Proper utilization of these vectors will help the voltages of the capacitors to achieve balance.

5. The Three-Level Converter

5.1SVM Under Voltage-Balanced Conditions

Suitable vectors from the SV diagram should be chosen for each modulation cycle in order to generate the reference vector (*m*). The vectors nearest to *m* are the most appropriate selections in terms of their ability to minimize the switching frequencies of the power devices, improve the quality of the output voltage spectra, and the electromagnetic interference (EMI).

In Fig19 ., the SV diagram of the three-level converter is divided into sextants, and each sextant is then divided into four triangular regions in order to show the vectors nearest to the reference.

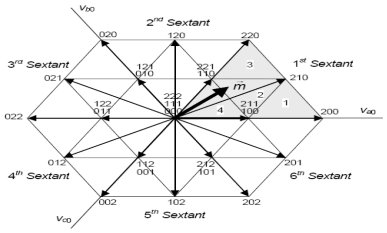


Fig.19

Three-level vector diagram divided into sextants and regions

Four groups of vectors can be distinguished in this diagram, as described in the following.

(1) The "large vectors" (200, 220, 020, 022, 002 and 202) assign the output voltages of the converter to either the highest or the lowest DC voltage levels. As they do not connect any output to the NP, they do not affect the voltage balance of the capacitors. These vectors can generate the highest

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AC voltage amplitudes because they have the greatest lengths. In fact, these six vectors are equivalent to the active ones of the two-level converter

(2) The "medium vectors" (210, 120, 021, 012, 102 and 201) connect each output to a different DC-link voltage level. Under balanced conditions, their tip end in the middle of the segments that join two consecutive large vectors. The length of the medium vectors defines the maximum amplitude of the reference vector for linear modulation and steady-state conditions, which is 3 2 the length of the large vectors. Since one output is always connected to the NP, the corresponding output current will define the NP current ($_{1i}$) . This connection produces voltage imbalances in the capacitors, and these must be compensated.

(3) The "short vectors" (100-211, 110-221, 010-121, 011-122, 001-112 and 101- 212) connect the AC outputs to two consecutive DC-link voltage levels. Their length is half the length of the large vectors. They are double vectors, which means that two states of the converter can generate the same voltage vector. As they affect the NP current in opposite ways, proper utilization of these vectors will help the NP voltage to achieve balance

(4) The "zero vectors" (000, 111 and 222) are in the origin of the diagram. They connect all of the outputs of the converter to the same DC-link voltage level, and therefore, they do not produce any current in the DC side.

5.2Applications:

Pulse width modulation (PWM) is a powerful technique for controlling analog circuits with a processor's digital outputs. PWM is employed in a wide variety of applications, ranging from measurement and communications to power control and conversion.

6. PWM Controller

Many microcontrollers include on-chip PWM controllers. For example, **Microchip**'s PIC16C67 includes two, each of which has a selectable on-time and period. The duty cycle is the ratio of the on-time to the period; the modulating frequency is the inverse of the period. To start PWM operation, the data sheet suggests the software should

- Set the period in the on-chip timer/counter that provides the modulating square wave
- Set the on-time in the PWM control register
- Set the direction of the PWM output, which is one of the general-purpose I/O pins
- Start the timer
- Enable the PWM controller

Although specific PWM controllers do vary in their programmatic details, the basic idea is generally the same

7.BLOCK DIAGRAM

Fig.20 shows a schematic drawing of a multilevel inverter using cascaded inverters with separated DC sources. Three-phase output voltage waveforms are generated by various switching combination of the switches in each Hbridge converter. Three levels at the output phase voltage waveforms are generated as +E/2, 0, -E/2 [5].

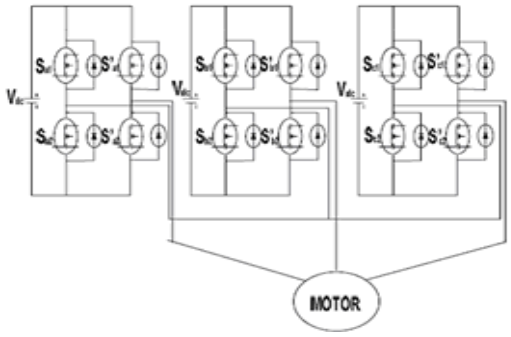
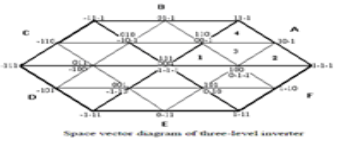


Fig 20 schematic diagram of a multilevel inverter

A three-level inverter is characterized by 33= 27 switching states as indicated in Fig.2 where the space vector diagram for the three-level inverter which is divided into the six sectors (A, B, C, D, E and F) is also shown. There are 24 active states, and three zero states that lie at the center of the hexagon. Each sector has four regions (1,2,3,4) [2]. The switching states of the inverter are summarized in Table I, where x represents the output phases, a, b and c [6- 7].

TABLE I
SWITCHING STATES OF THE INVERTER SWITCHES (X=A, B, C PHASES)

V_{x0}	S_{X1}	S_{X2}	S_{X1}	S_{X2}
$V_{dc}/2$	1	0	0	1
0	1	1	0	0
0	0	1	0	1
$-V_{dc}/2$	0	1	1	0



Space vector diagram of three-level inverter

The principle of SVPWM method is that the command voltage vector is approximately calculated by using three adjacent vectors. The duration of each voltage vectors
obtained by vector calculations;

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$$T1V1+T2V2+T3V3=TsV^* \quad (12)$$
$$T1+T2+T3=Ts$$

where V1, V2, and V3 are vectors that define the triangle region in which V* is located. T1, T2 and T3 are the corresponding vector durations and Ts is the sampling time. In a three-level inverter similar to a two-level inverter, each space vector diagram is divided into 6 sectors.

7.1 COMPUTER MODEL

Fig. shows Simulink model of the whole system including a three-phase induction motor load. "Sector Determination" block in Fig.7 calculates α and amplitude of the command vector V* according to the demand inverter output frequency and modulation index. Then, the sector is found

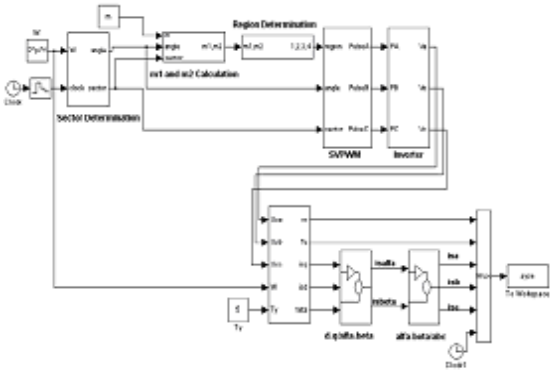

Fig 21 Simulink model of the whole system

using by the value of α. "m1 and m2 Calculation" block is used to calculate m1 and m2 vectors using (2-4). "Region Determination" block in Fig.7 obtains the region in which the vector falls into according to rules given in Subsection B. "SVPWM" block calculates the switching times according to Table.2 and generates SVPWM signals as explained in Subsection D. "Inverter" block represents the three-phase inverter model using ideal switches. Induction motor is modeled as shown in Fig.7 with three separated blocks. However, R-L load model is not shown here.

8. SIMULATION RESULTS FROM THREE-LEVEL INVERTER

Simulation results have been taken for various operating conditions feeding a passive load for R=100Ω and L=0.1H

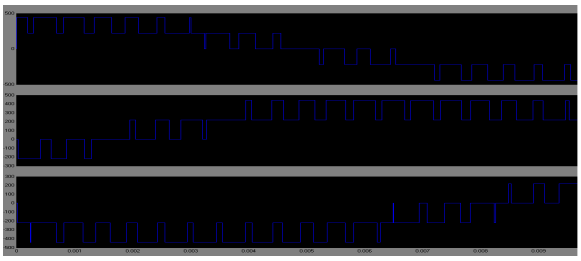

Fig.22 OUTPUT WAVEFORM FOR PHASE VOLTAGE

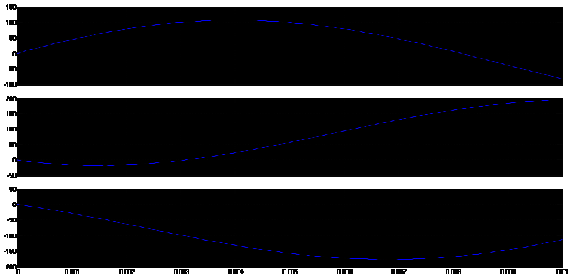

Fig.23 out put waveform for Three-Phase line current

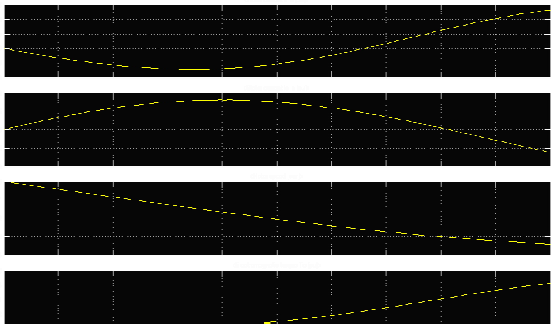

Fig.24 Output Waveforms for rotor current Ir, stator current Is, rotor speed, electromagnetic torque

9. CONCLUSION

The space vector PWM algorithm for a three level voltage-fed inverter using cascaded H-bridges inverter has been modeled and simulated using Simulink/MATLAB package program. Simulation results have been given for both R-L and induction motor loads using 1kHz switching frequency with various output frequencies. The proposed control algorithm used in the three-level inverter can be easily applied to multilevel inverters with more than three levels. It has been shown that high quality waveforms at the output of the multilevel inverter can be obtained even with 1kHz of low switching frequency.

APPENDIX

Ratings of the three-phase, 4-pole, 380 V, 50 Hz squirrel cage induction motor are:
Frequency range: 0-65Hz
Stator resistance (Rs): 7Ω
Rotor resistance (Rr): 6Ω
Stator leak. inductance (Lls): 0.52mH
Rotor leak. inductance (Llr): 0.52mH
Magnetizing inductance (Lm): 0.5mH
Rotor inertia(J):0.0085

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